

8

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

PAGE

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23

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24

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25

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36

SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK

37

SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF

38

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39

FUNCTIONAL TEST POINTS

40

REVISION HISTORY (1 OF 1)

41-42

SIGNAL NAMES

43-44

COMPONENT LOCATIONS

REV

ZONE

ECN

DESCRIPTION OF CHANGE

CK APPD
DATE

ENG APPD
DATE

01

308060

ENGINEERING RELEASED

12/19/03

?

SINCLAIR Q41A

12/18/2003

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS		✓
INT_TMDS	✓	
NO_4XVCORE	✓	

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

BOM OPTION

051-6598

1

SCHEM,MLB,Q41A

SCH1

820-1615

1

PCBF,MLB,Q41A

PCB1

DIMENSIONS ARE IN MILLIMETERS


XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING



THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD


DESIGNER

SCALE

SIZE

D

MATERIAL/FINISH NOTED AS APPLICABLE

 Apple Computer Inc.

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TITLE

SCHEM,MLB,Q41A

DRAWING NUMBER

051-6598

REV.

01

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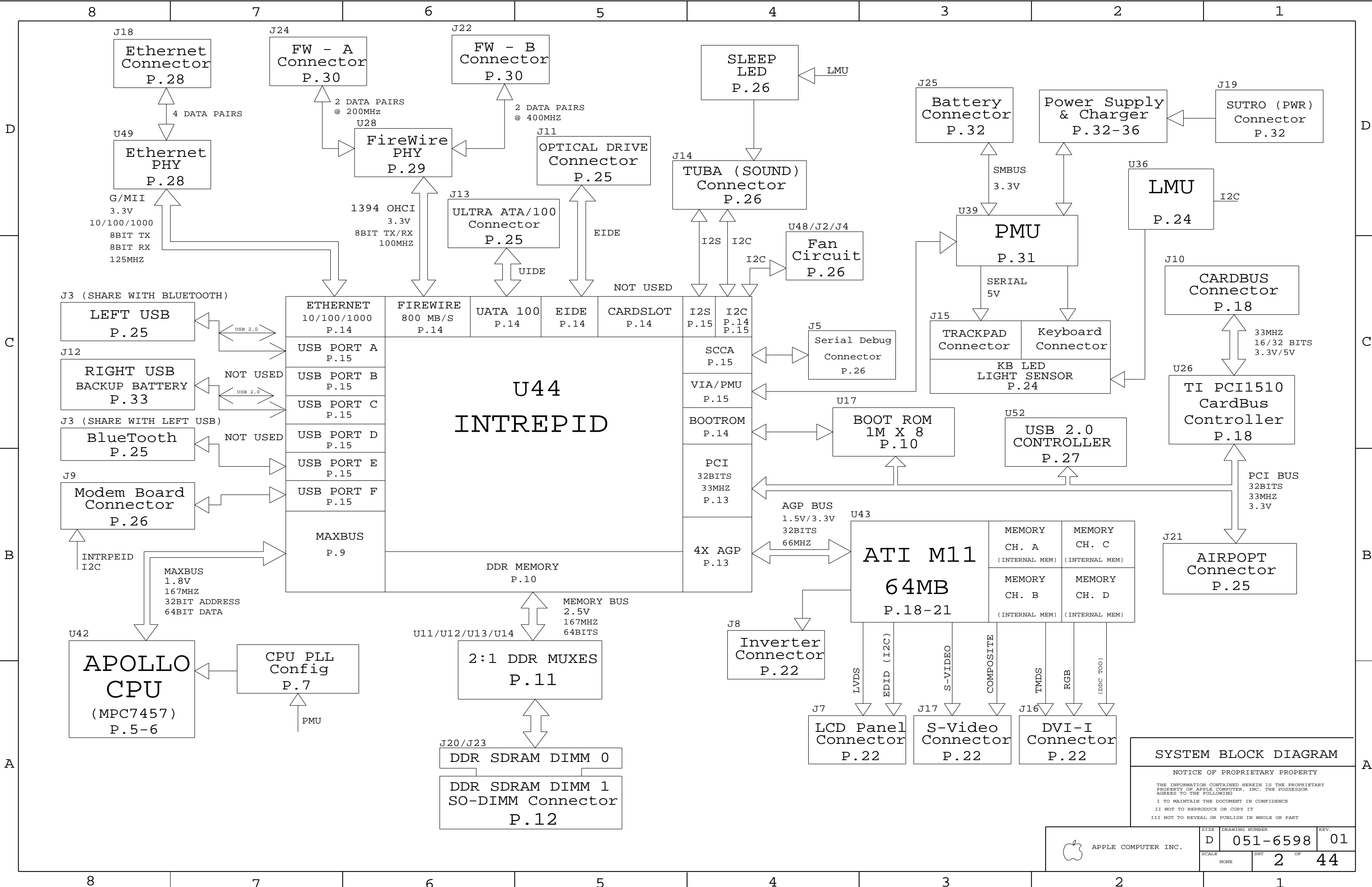
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SYSTEM BLOCK DIAGRAM

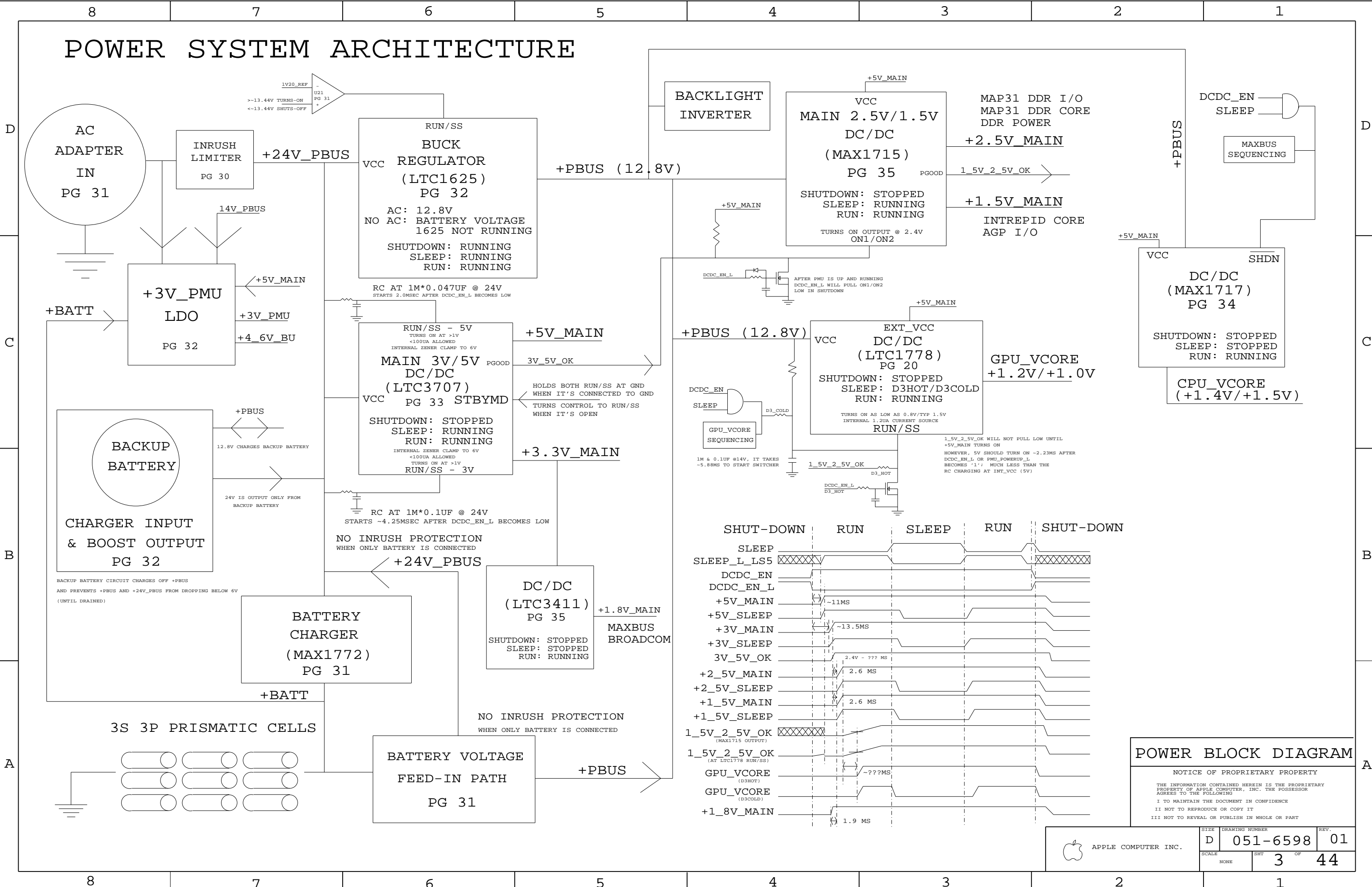
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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

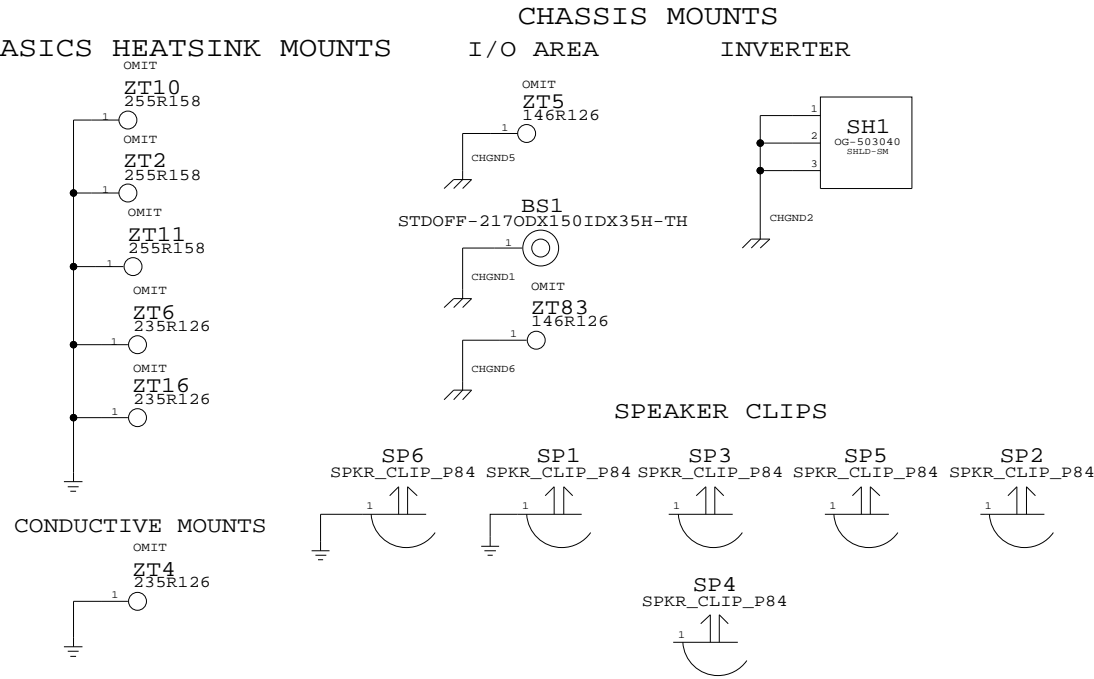
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

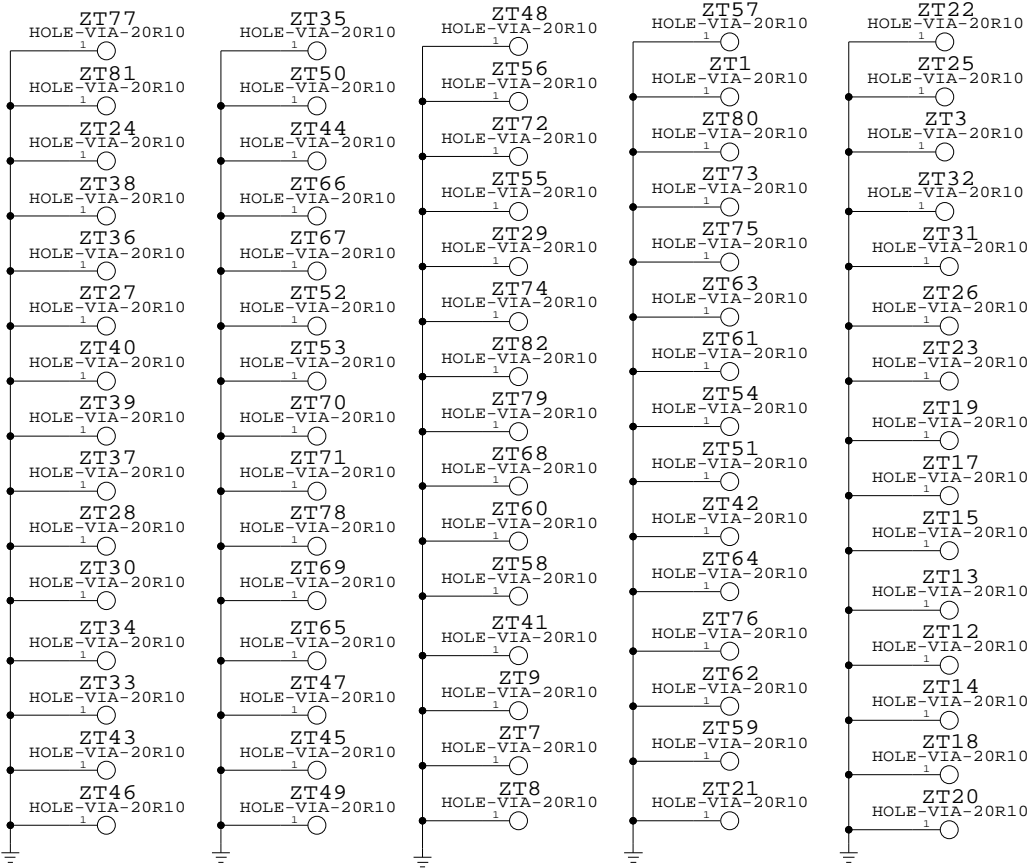
20R10 TH VIA OR VIA IN PAD

1	SIGNAL (1/3 OZ + COPPER PLATING)	
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



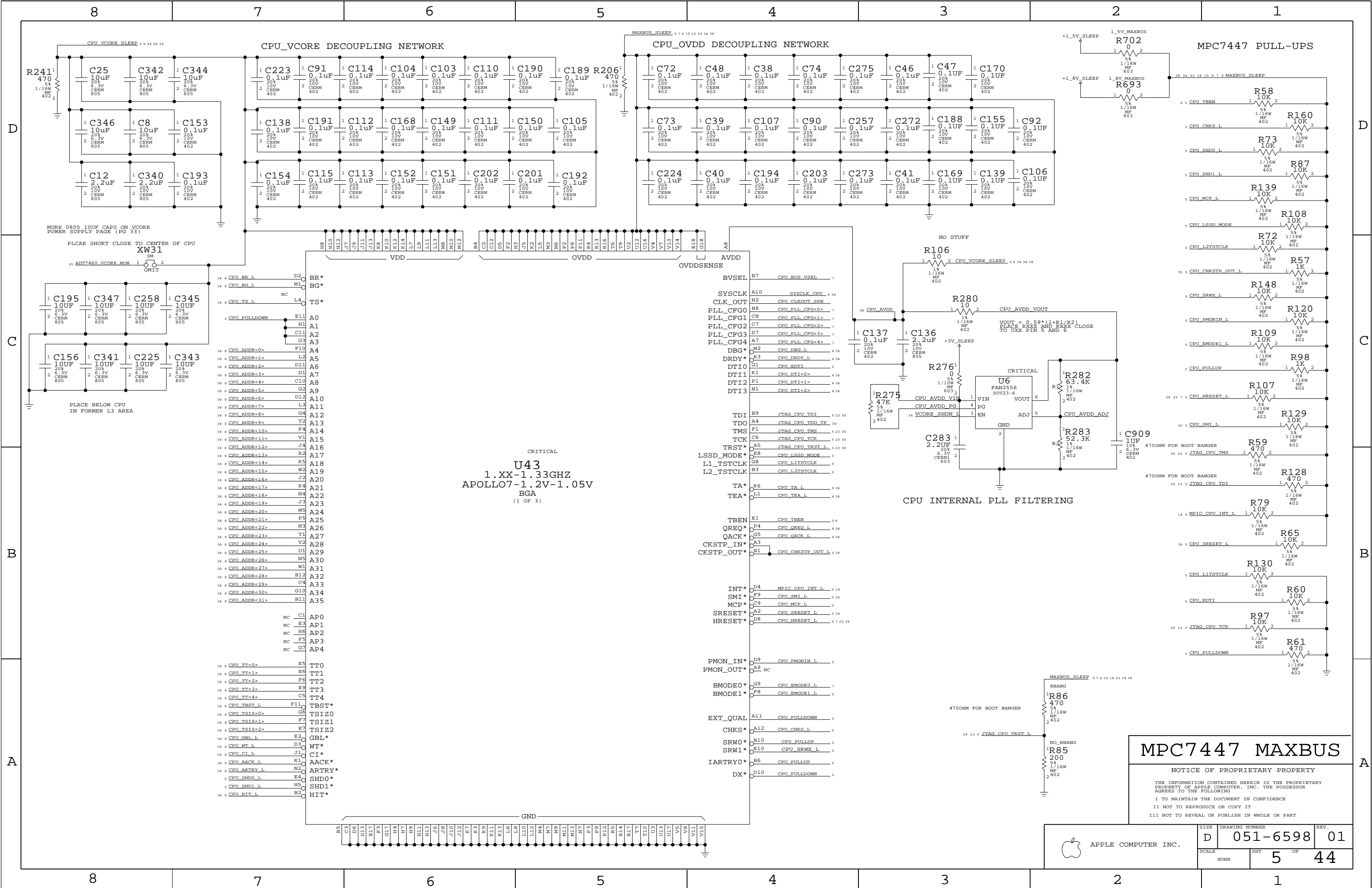
BOARD INFORMATION

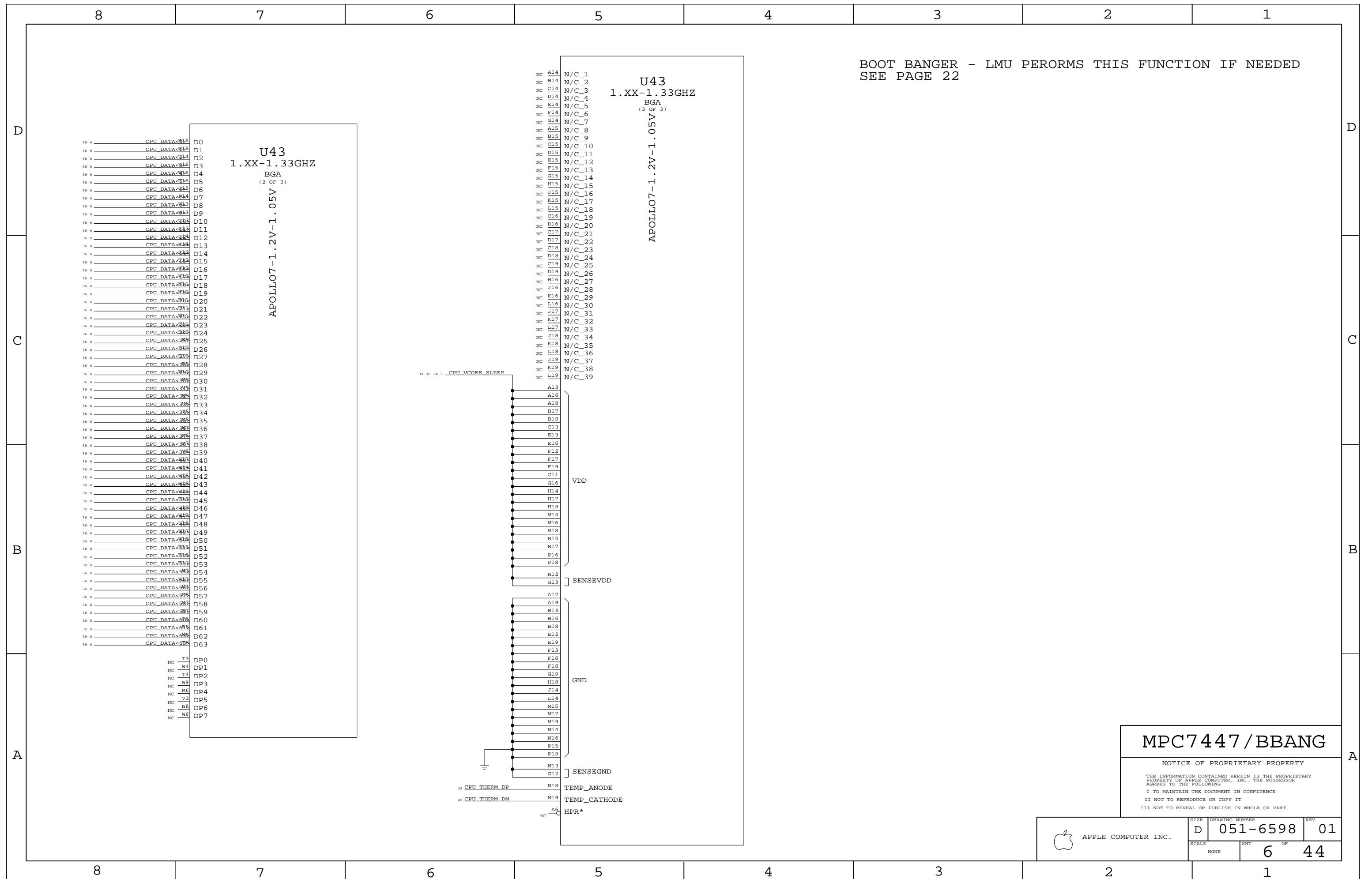
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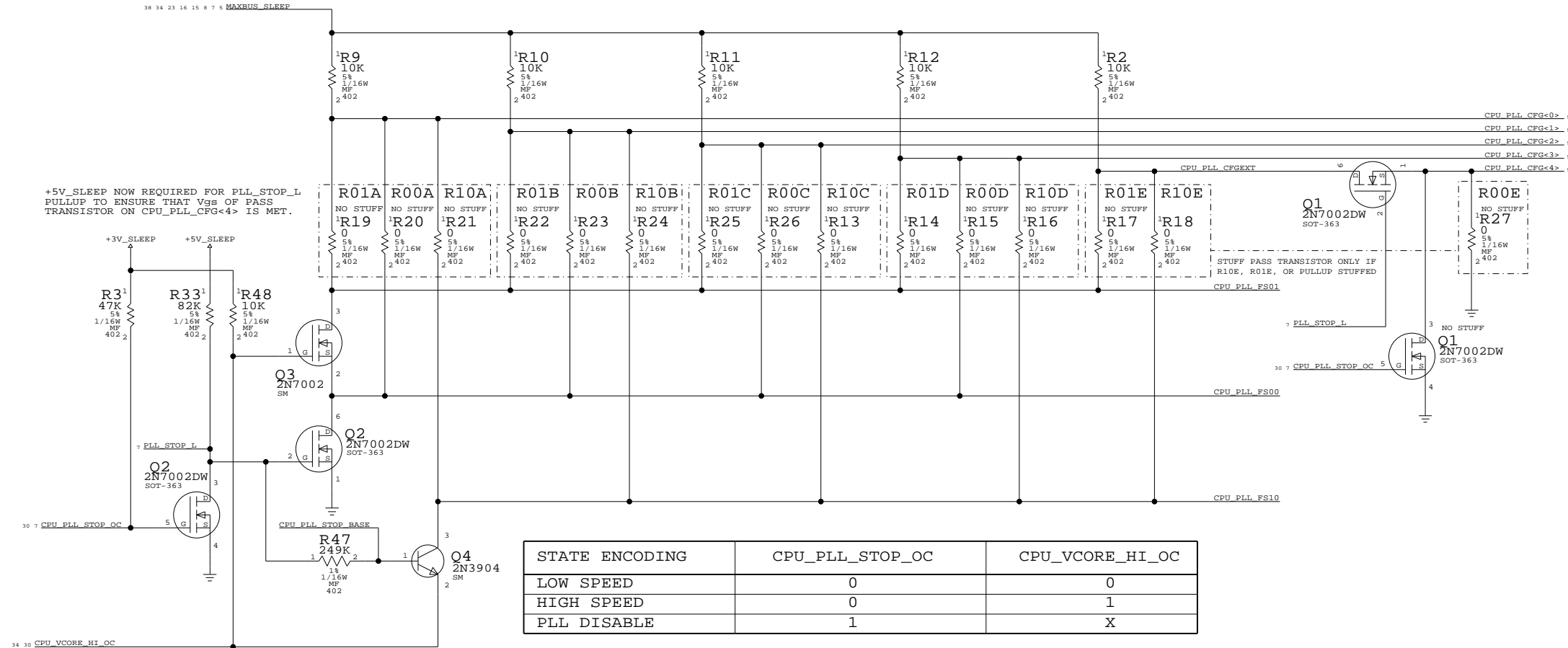
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D	051-6598	01
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NONE	4	44





CPU PLL CONFIG CIRCUITRY

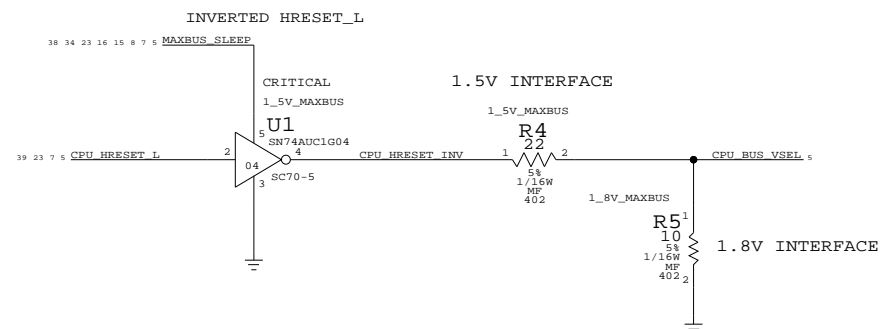
CPU FREQUENCY CONFIGURATION



MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ 133MHZ		CPU_PLL_CFG		
	(MHZ)		4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

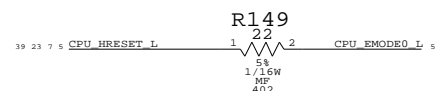
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING
INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION


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	SCALE	SHT	OF
	NONE	7	44

INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

- 1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D46 - SELPCIISPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

INTREPID BOOT STRAPS

BIT 56 TO 63

Intrepid MaxBus

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SCALE: NONE SHIT: 8 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

BIT 56 TO 63

INTREPID BOOT STRAPS

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D 051-6598 REV. 01

SCALE NONE SHT 8 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

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INTREPID BOOT STRAPS

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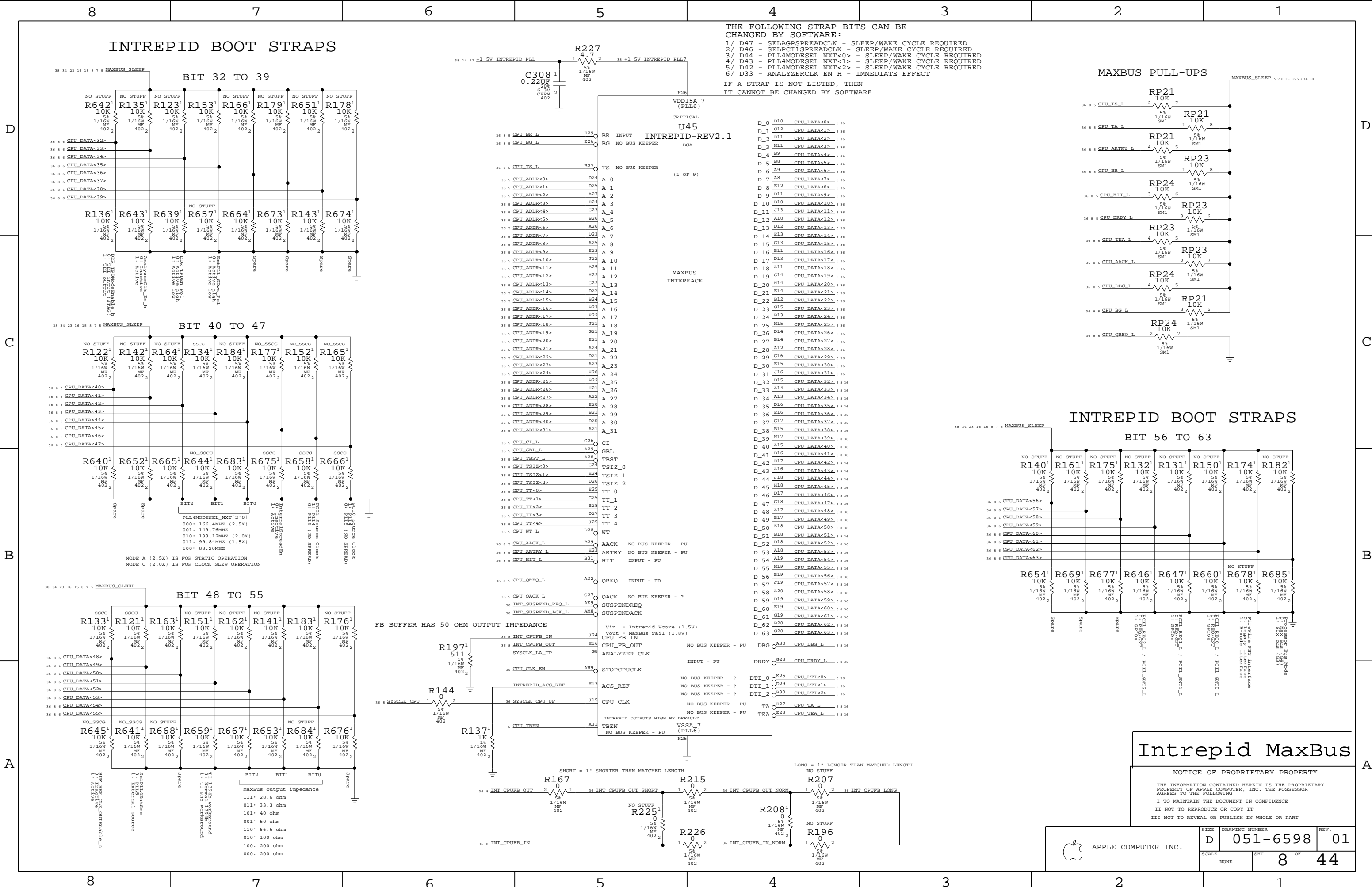
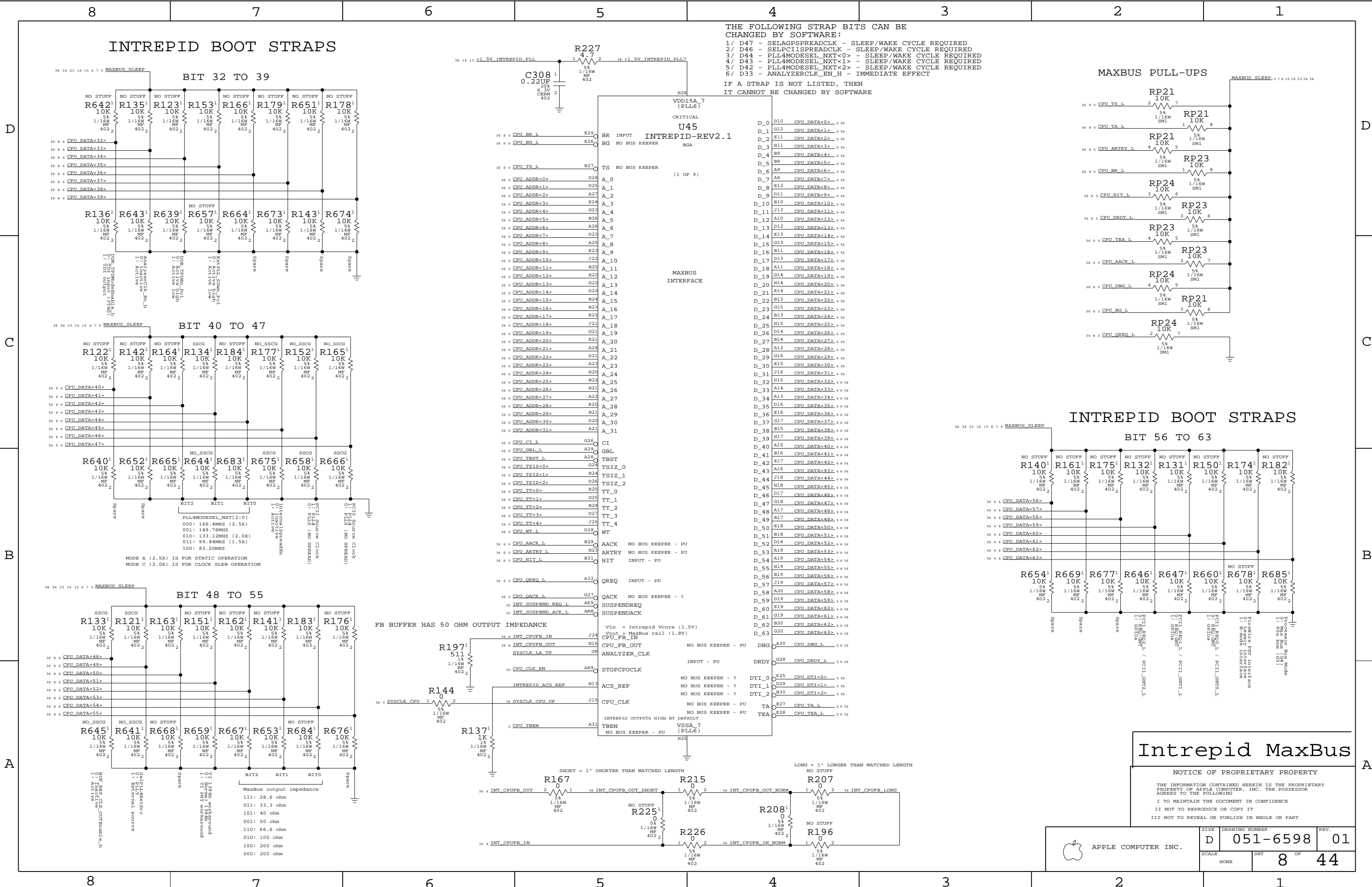
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APPLE COMPUTER INC.

D 051-6598 REV. 01

SCALE NONE SHT 8 OF 44

[illegible]

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MAXBUS PULL-UPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

BIT 56 TO 63

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INTREPID ACS REF

INTREPID OUTPUTS HIGH BY DEFAULT

SHORT = 1" SHORTER THAN MATCHED LENGTH

LONG = 1" LONGER THAN MATCHED LENGTH

PIN	SIGNAL	FUNCTION
D_0	D10	CPU_DATA<0>
D_1	G12	CPU_DATA<1>
D_2	E11	CPU_DATA<2>
D_3	H11	CPU_DATA<3>
D_4	B9	CPU_DATA<4>
D_5	B8	CPU_DATA<5>
D_6	A9	CPU_DATA<6>
D_7	E12	CPU_DATA<7>
D_8	E12	CPU_DATA<8>
D_9	D11	CPU_DATA<9>
D_10	B10	CPU_DATA<10>
D_11	J13	CPU_DATA<11>
D_12	A10	CPU_DATA<12>
D_13	D12	CPU_DATA<13>
D_14	E13	CPU_DATA<14>
D_15	G13	CPU_DATA<15>
D_16	B11	CPU_DATA<16>
D_17	D13	CPU_DATA<17>
D_18	A11	CPU_DATA<18>
D_19	G14	CPU_DATA<19>
D_20	H14	CPU_DATA<20>
D_21	E14	CPU_DATA<21>
D_22	B12	CPU_DATA<22>
D_23	G15	CPU_DATA<23>
D_24	B13	CPU_DATA<24>
D_25	H15	CPU_DATA<25>
D_26	D14	CPU_DATA<26>
D_27	B14	CPU_DATA<27>
D_28	A12	CPU_DATA<28>
D_29	G16	CPU_DATA<29>
D_30	E15	CPU_DATA<30>
D_31	J16	CPU_DATA<31>
D_32	D15	CPU_DATA<32>
D_33	A14	CPU_DATA<33>
D_34	A13	CPU_DATA<34>
D_35	D16	CPU_DATA<35>
D_36	E16	CPU_DATA<36>
D_37	G17	CPU_DATA<37>
D_38	B15	CPU_DATA<38>
D_39	H17	CPU_DATA<39>
D_40	A15	CPU_DATA<40>
D_41	B16	CPU_DATA<41>
D_42	E17	CPU_DATA<42>
D_43	A16	CPU_DATA<43>
D_44	J18	CPU_DATA<44>
D_45	H18	CPU_DATA<45>
D_46	D17	CPU_DATA<46>
D_47	G18	CPU_DATA<47>
D_48	A17	CPU_DATA<48>
D_49	B17	CPU_DATA<49>
D_50	E18	CPU_DATA<50>
D_51	B18	CPU_DATA<51>
D_52	D18	CPU_DATA<52>
D_53	A18	CPU_DATA<53>
D_54	A19	CPU_DATA<54>
D_55	H19	CPU_DATA<55>
D_56	B19	CPU_DATA<56>
D_57	J19	CPU_DATA<57>
D_58	A20	CPU_DATA<58>
D_59	D19	CPU_DATA<59>
D_60	E19	CPU_DATA<60>
D_61	G19	CPU_DATA<61>
D_62	R20	CPU_DATA<62>
D_63	G20	CPU_DATA<63>
DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L
QACK	G27	NO BUS KEEPER - ?
SUSPENDREQ	AK9	NO BUS KEEPER - ?
SUSPENDACK	AM8	NO BUS KEEPER - ?
Vin	-	Intrepid Vcore (1.5V)
Vout	-	Maxbus rail (1.8V)
CPU_FB_IN	-	NO BUS KEEPER - PU
CPU_FB_OUT	-	NO BUS KEEPER - PU
SYSCLK_LA_TP	-	ANALYZER_CLK
CPU_CLK_EN	AH9	STOPCPUCLK
ACS_REF	H13	NO BUS KEEPER - ?
CPU_CLK	J15	NO BUS KEEPER - ?
TBEN	A32	NO BUS KEEPER - PU
INT_CPUFB_IN	-	NO BUS KEEPER - PU
INT_CPUFB_OUT	-	NO BUS KEEPER - PU
INT_CPUFB_OUT_SHORT	-	NO BUS KEEPER - PU
INT_CPUFB_OUT_NORM	-	NO BUS KEEPER - PU
INT_CPUFB_LONG	-	NO BUS KEEPER - PU

Intrepid MaxBus

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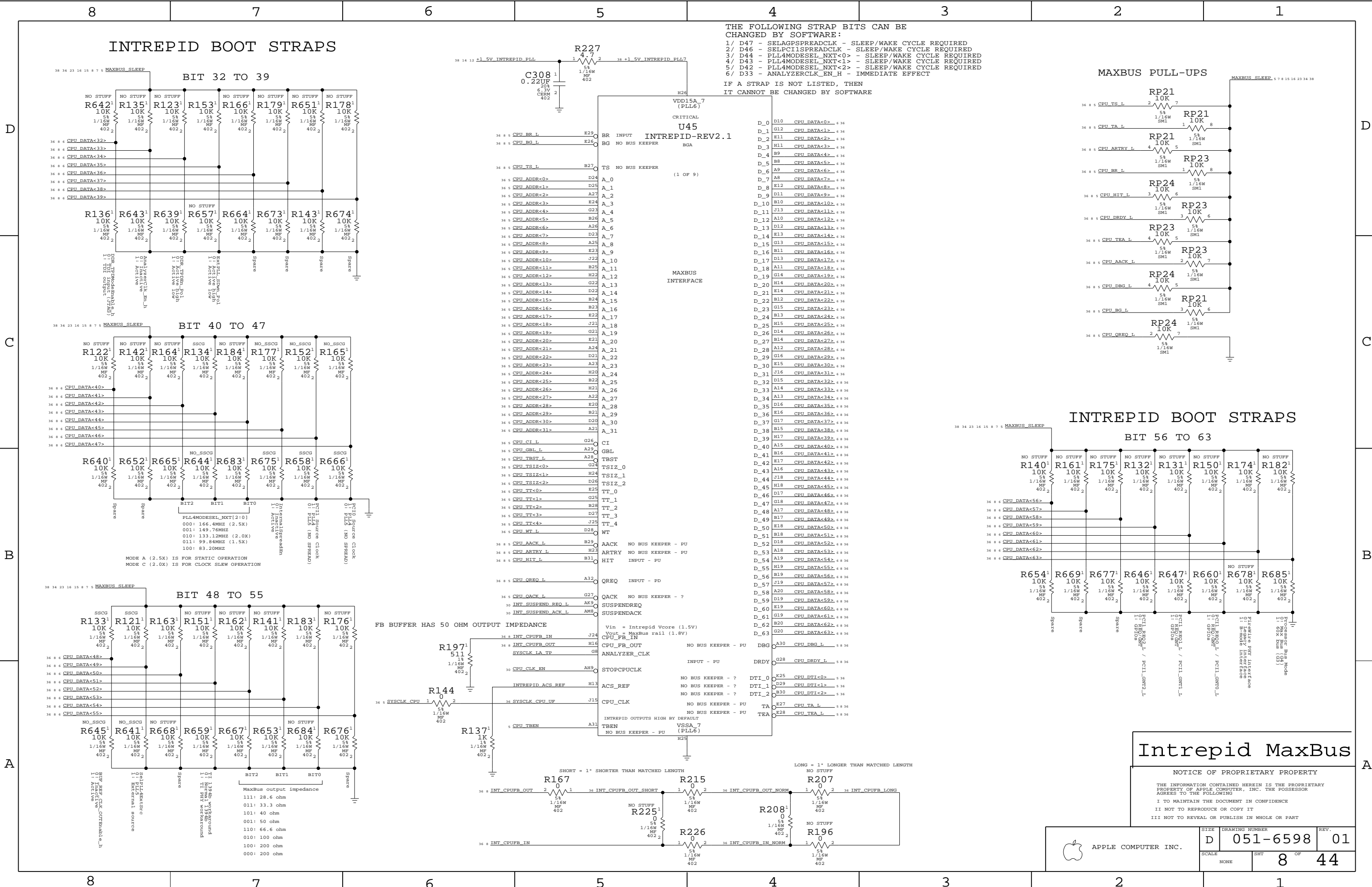
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REV.: 01

SCALE: NONE

SHT: 8 OF 44

[illegible]

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D_4	B9	CPU_DATA<4>
D_5	B8	CPU_DATA<5>
D_6	A9	CPU_DATA<6>
D_7	E12	CPU_DATA<7>
D_8	E12	CPU_DATA<8>
D_9	D11	CPU_DATA<9>
D_10	B10	CPU_DATA<10>
D_11	J13	CPU_DATA<11>
D_12	A10	CPU_DATA<12>
D_13	D12	CPU_DATA<13>
D_14	E13	CPU_DATA<14>
D_15	G13	CPU_DATA<15>
D_16	B11	CPU_DATA<16>
D_17	D13	CPU_DATA<17>
D_18	A11	CPU_DATA<18>
D_19	G14	CPU_DATA<19>
D_20	H14	CPU_DATA<20>
D_21	E14	CPU_DATA<21>
D_22	B12	CPU_DATA<22>
D_23	G15	CPU_DATA<23>
D_24	B13	CPU_DATA<24>
D_25	H15	CPU_DATA<25>
D_26	D14	CPU_DATA<26>
D_27	B14	CPU_DATA<27>
D_28	A12	CPU_DATA<28>
D_29	G16	CPU_DATA<29>
D_30	E15	CPU_DATA<30>
D_31	J16	CPU_DATA<31>
D_32	D15	CPU_DATA<32>
D_33	A14	CPU_DATA<33>
D_34	A13	CPU_DATA<34>
D_35	D16	CPU_DATA<35>
D_36	E16	CPU_DATA<36>
D_37	G17	CPU_DATA<37>
D_38	B15	CPU_DATA<38>
D_39	H17	CPU_DATA<39>
D_40	A15	CPU_DATA<40>
D_41	B16	CPU_DATA<41>
D_42	E17	CPU_DATA<42>
D_43	A16	CPU_DATA<43>
D_44	J18	CPU_DATA<44>
D_45	H18	CPU_DATA<45>
D_46	D17	CPU_DATA<46>
D_47	G18	CPU_DATA<47>
D_48	A17	CPU_DATA<48>
D_49	B17	CPU_DATA<49>
D_50	E18	CPU_DATA<50>
D_51	B18	CPU_DATA<51>
D_52	D18	CPU_DATA<52>
D_53	A18	CPU_DATA<53>
D_54	A19	CPU_DATA<54>
D_55	H19	CPU_DATA<55>
D_56	B19	CPU_DATA<56>
D_57	J19	CPU_DATA<57>
D_58	A20	CPU_DATA<58>
D_59	D19	CPU_DATA<59>
D_60	E19	CPU_DATA<60>
D_61	G19	CPU_DATA<61>
D_62	R20	CPU_DATA<62>
D_63	G20	CPU_DATA<63>
DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L
QACK	G27	NO BUS KEEPER - ?
SUSPENDREQ	AK9	NO BUS KEEPER - ?
SUSPENDACK	AM8	NO BUS KEEPER - ?
Vin		Intrepid Vcore (1.5V)
Vout		Maxbus rail (1.8V)
CPU_FB_IN		NO BUS KEEPER - PU
CPU_FB_OUT		NO BUS KEEPER - PU
SYSCLK_LA_TP		ANALYZER_CLK
CPU_CLK_EN	AH9	STOPCPUCLK
ACS_REF	H13	NO BUS KEEPER - ?
CPU_CLK	J15	NO BUS KEEPER - ?
TBEN	A32	NO BUS KEEPER - PU
QREQ	A32	INPUT - PD
CPU_QACK_L	G27	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	NO BUS KEEPER - ?
INT_SUSPEND_ACK_L	AM8	NO BUS KEEPER - ?
INT_CPUFB_IN		NO BUS KEEPER - PU
INT_CPUFB_OUT		NO BUS KEEPER - PU
INT_CPUFB_OUT_SHORT		NO BUS KEEPER - PU
INT_CPUFB_OUT_NORM		NO BUS KEEPER - PU
INT_CPUFB_IN_NORM		NO BUS KEEPER - PU

Intrepid MaxBus

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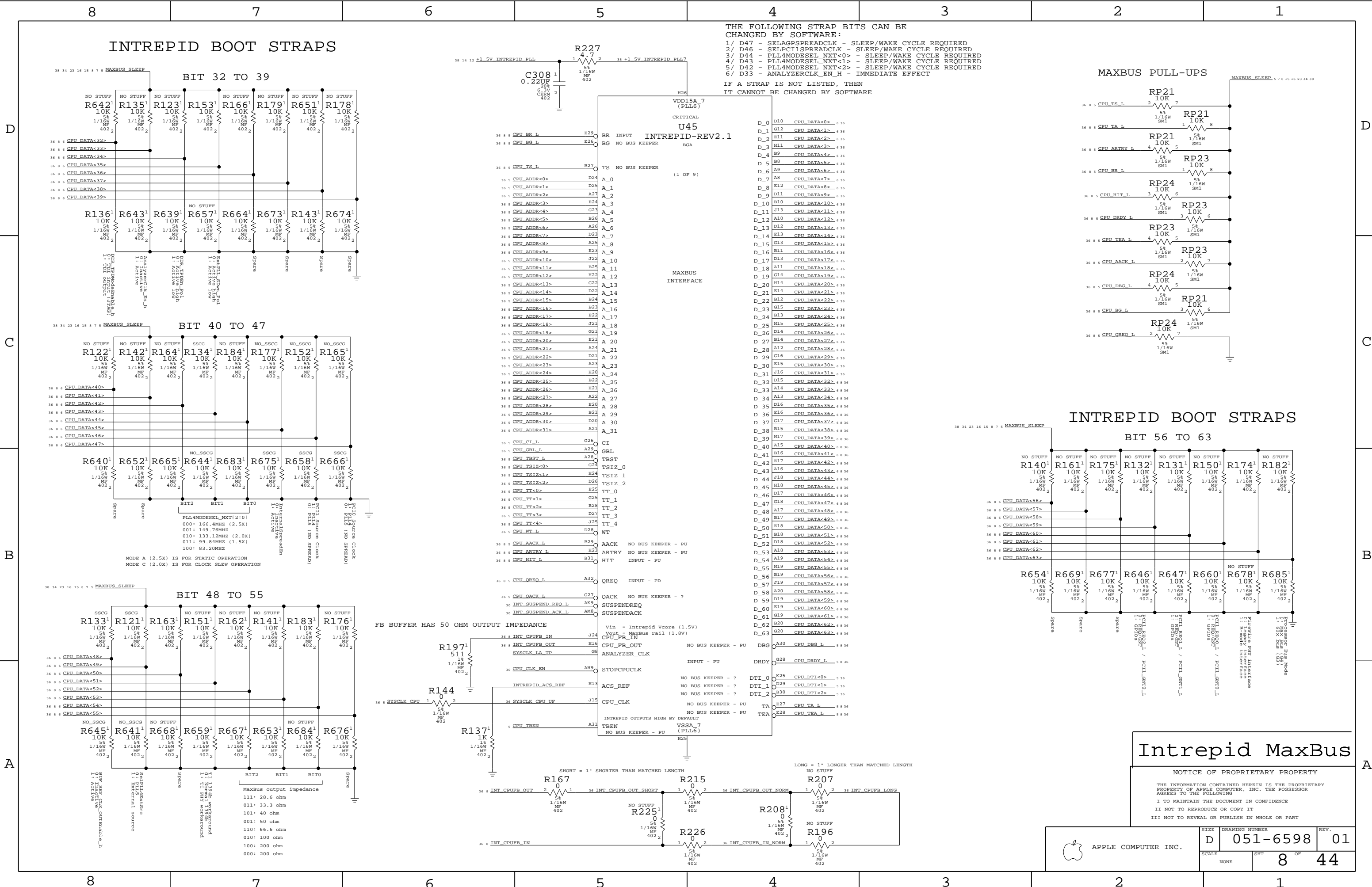
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APPLE COMPUTER INC.

D 051-6598 REV. 01

SCALE NONE SHEET 8 OF 44



INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

BIT 56 TO 63

INTREPID BOOT STRAPS

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D 051-6598 REV. 01

SCALE NONE SHT 8 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

BIT 56 TO 63

INTREPID BOOT STRAPS

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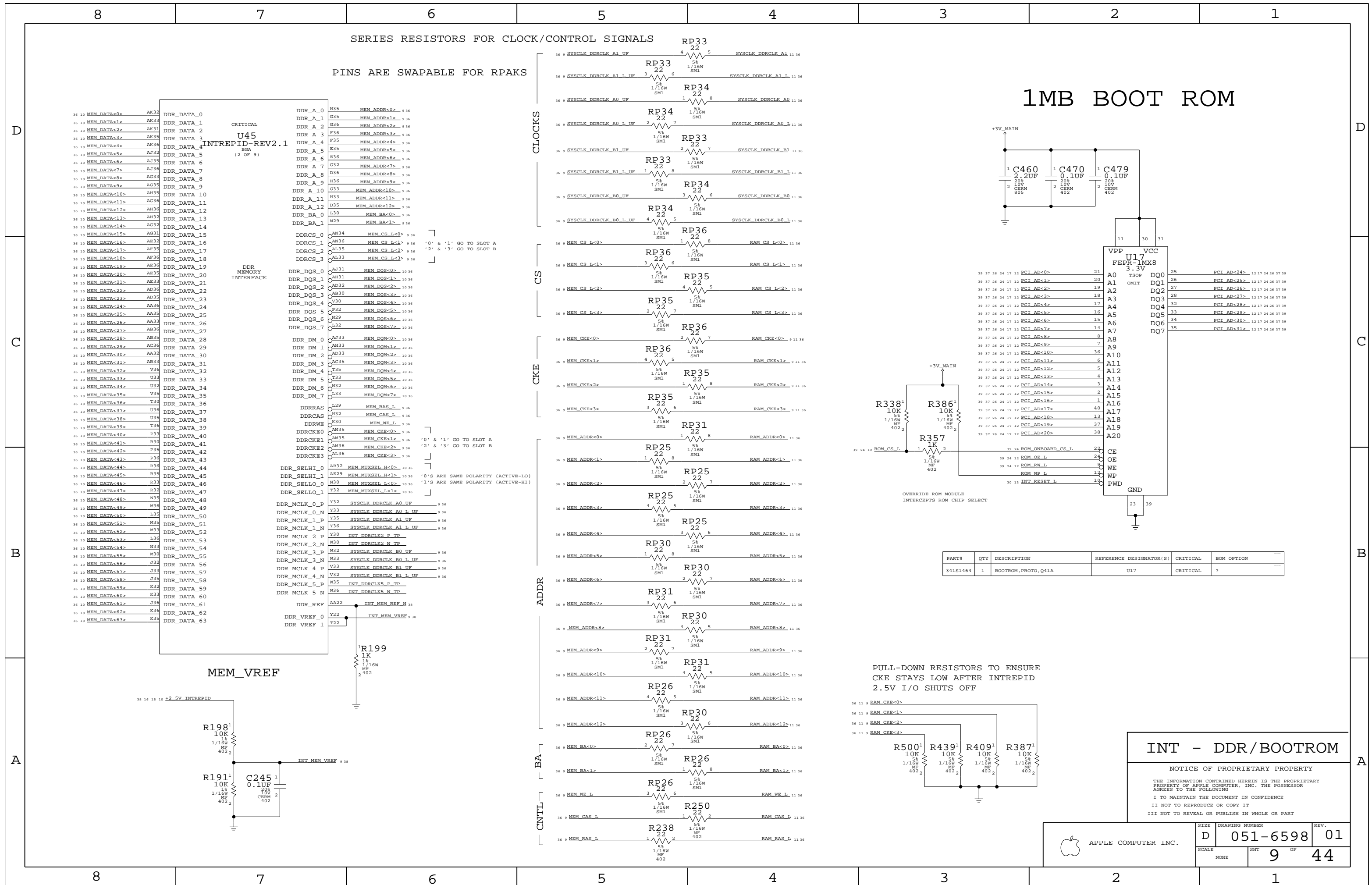
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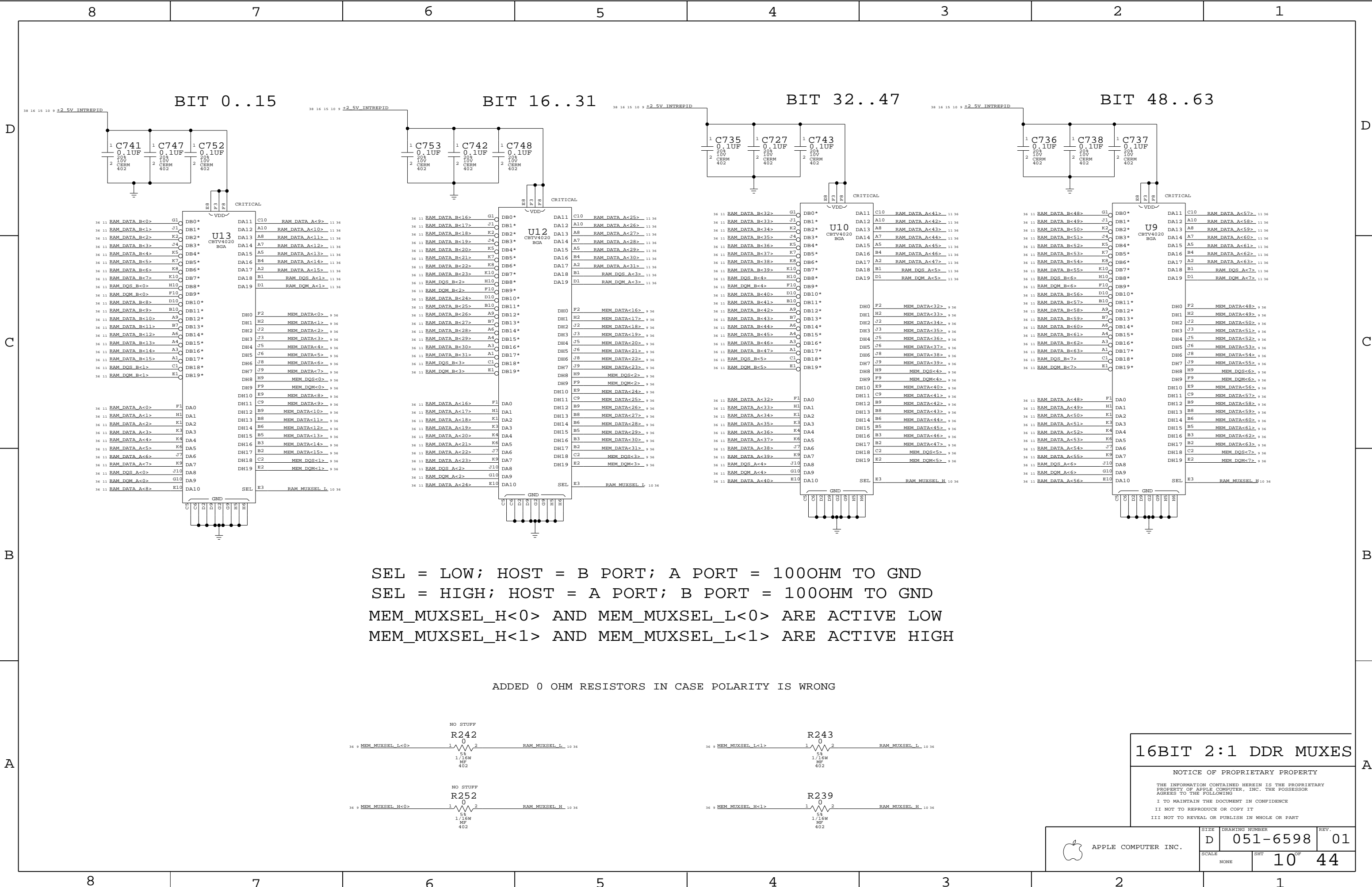
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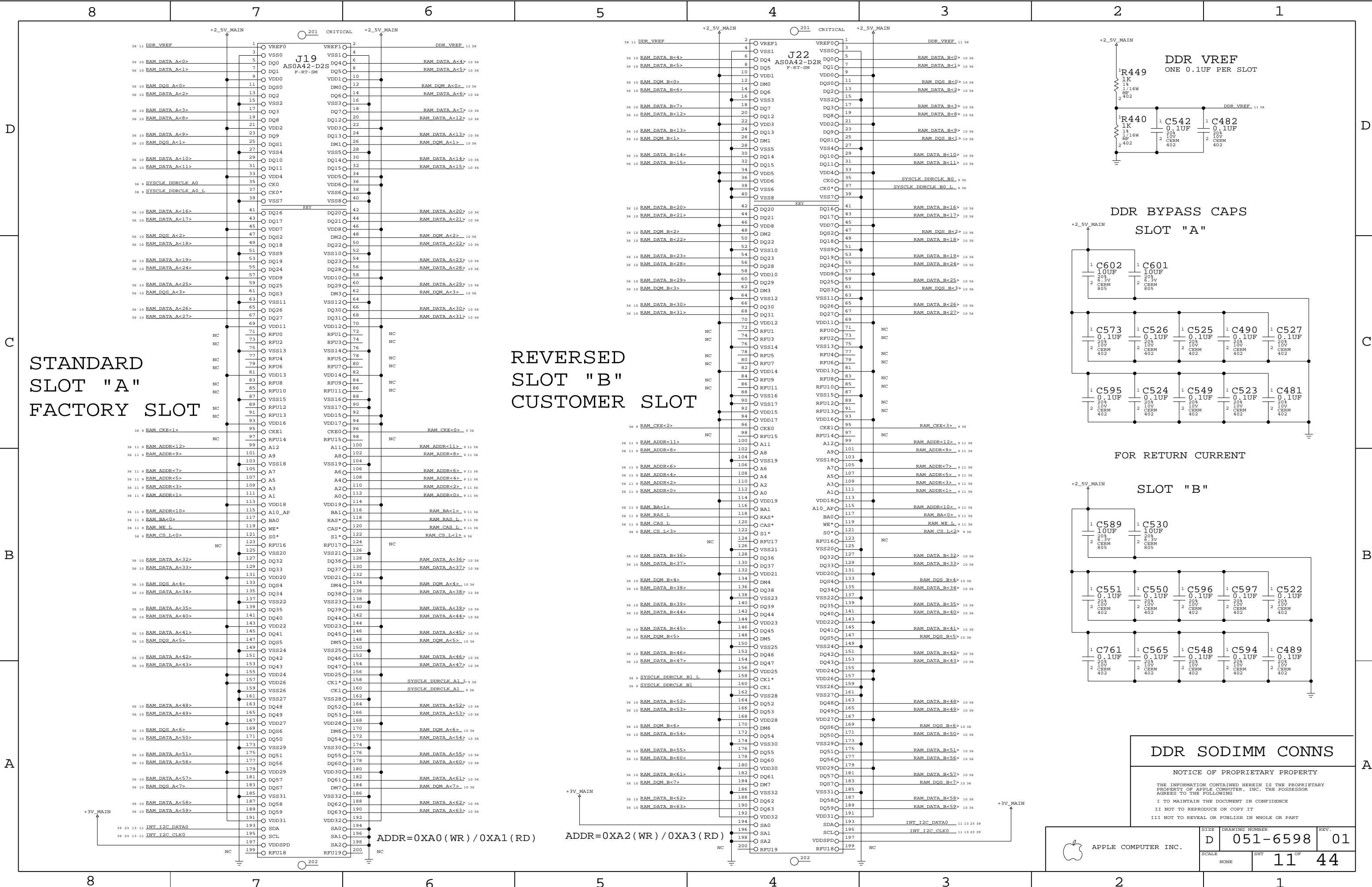
APPLE COMPUTER INC.

D 051-6598 REV. 01

SCALE NONE SHT 8 OF 44







STANDARD
SLOT "A"
FACTORY SLOT

REVERSED
SLOT "B"
CUSTOMER SLOT

DDR VREF
ONE 0.1UF PER SLOT

DDR BYPASS CAPS
SLOT "A"

FOR RETURN CURRENT

SLOT "B"

DDR SODIMM CONNS

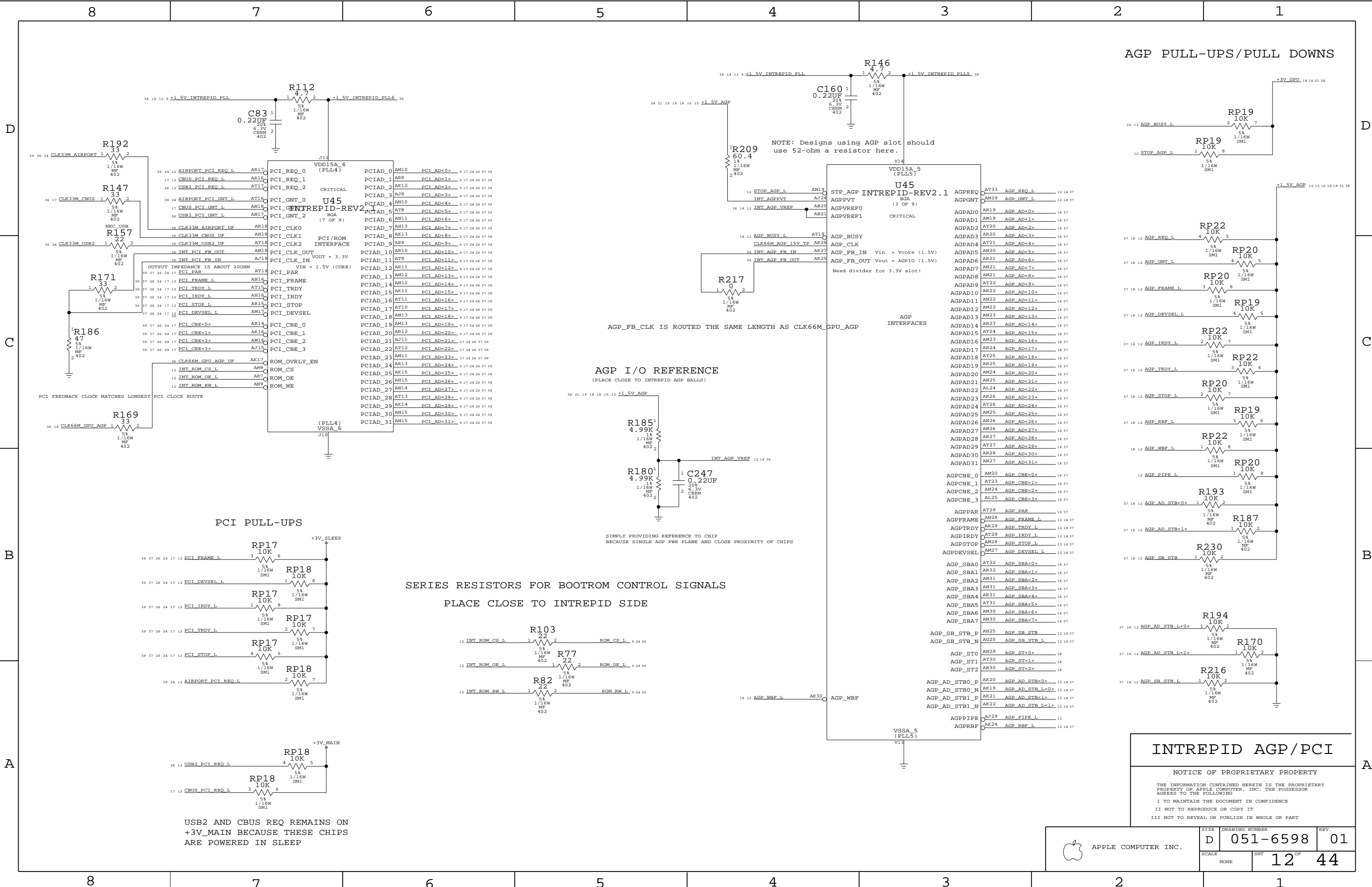
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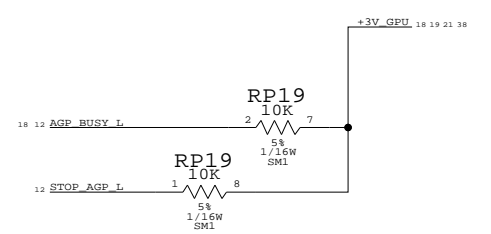


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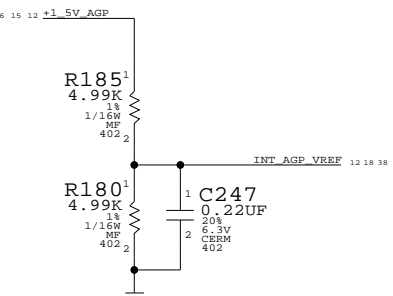
SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE	SHT	
NONE	11 ^{OF}	44



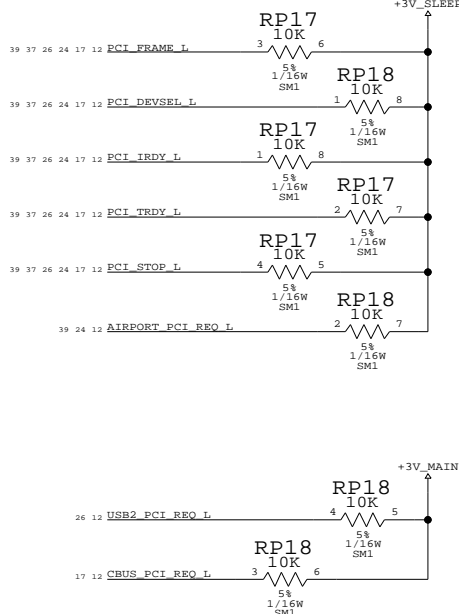
AGP PULL-UPS/PULL DOWNS



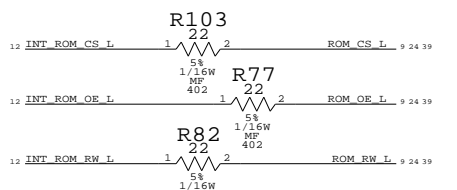
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)



PCI PULL-UPS



SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE



INTREPID AGP/PCI

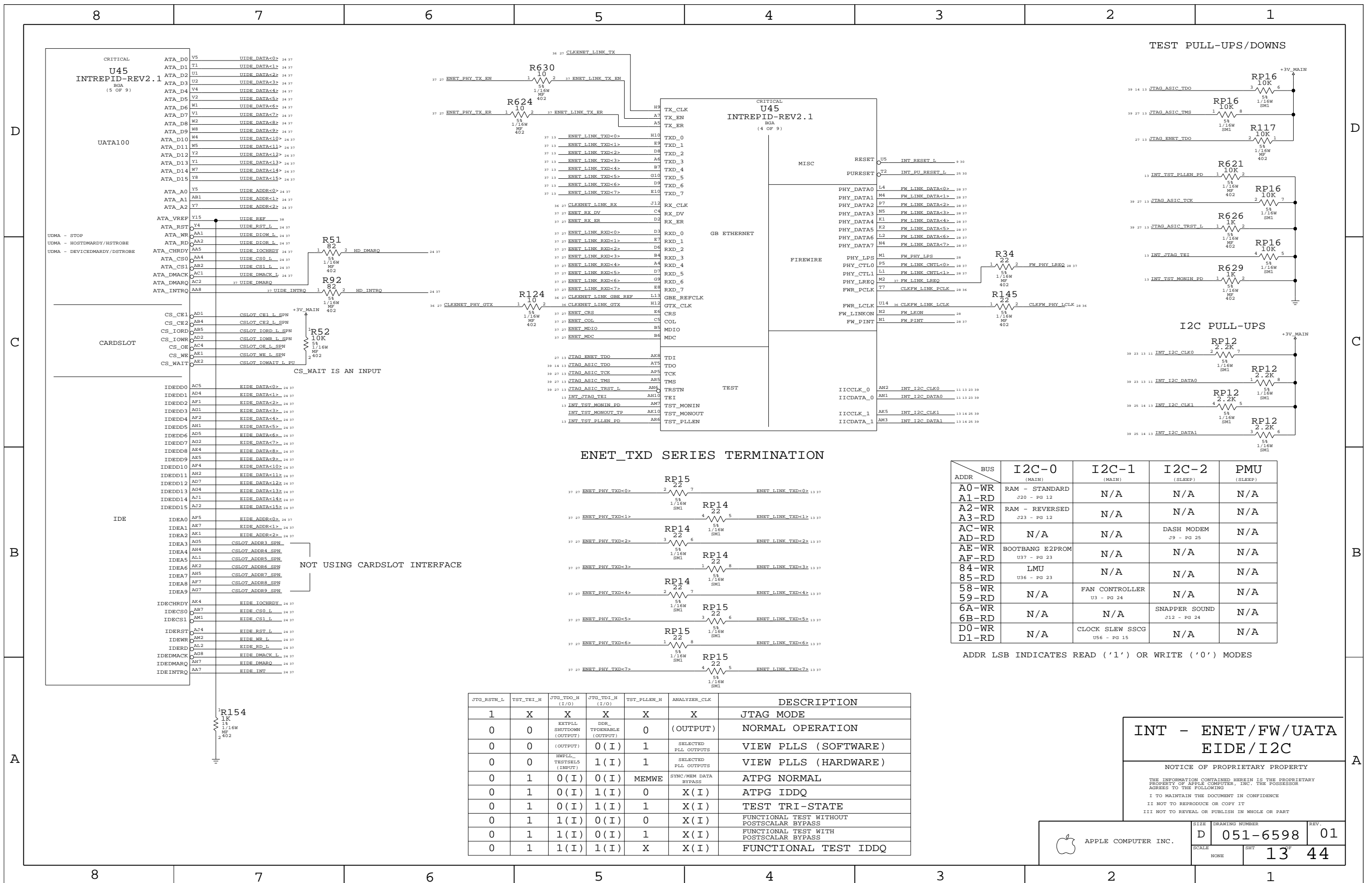
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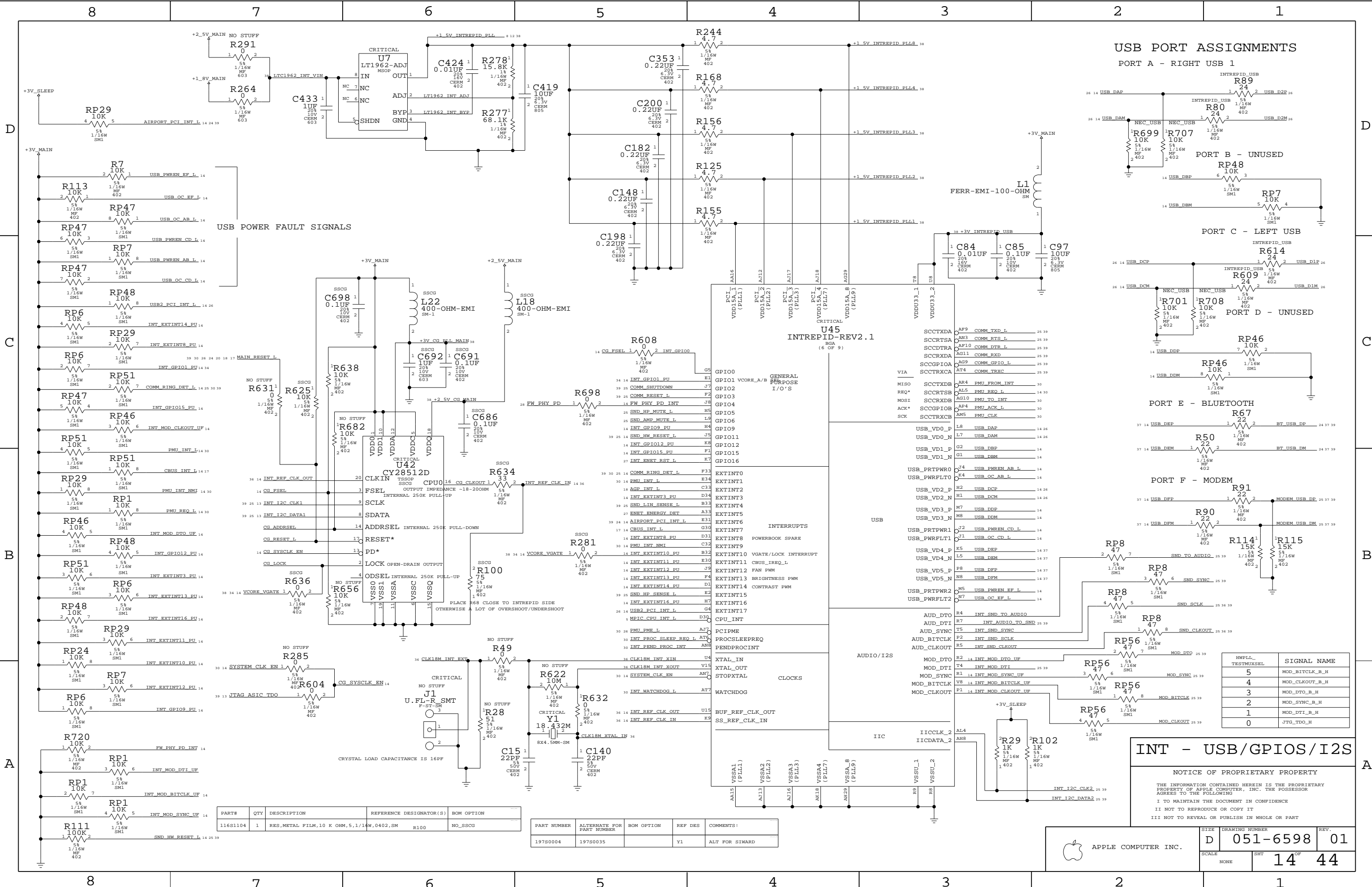
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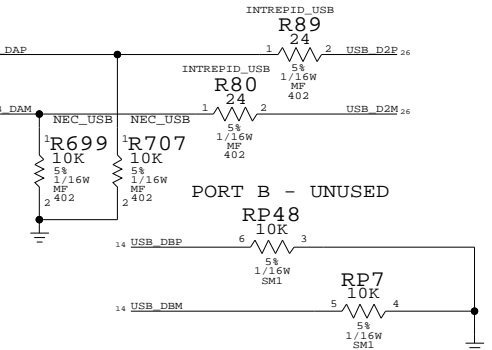
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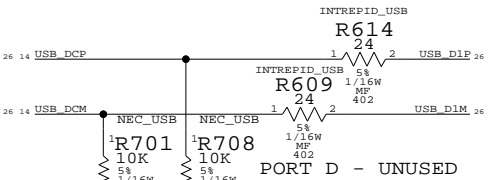


USB PORT ASSIGNMENTS

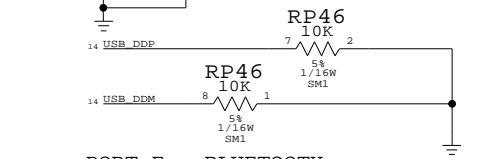
PORT A - RIGHT USB 1



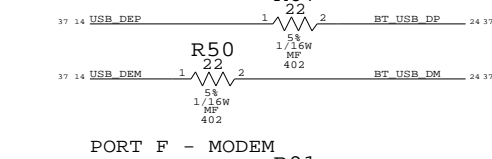
PORT B - UNUSED



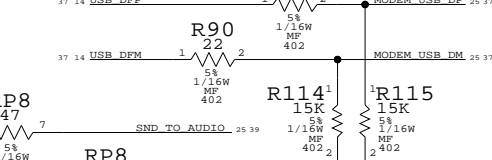
PORT C - LEFT USB



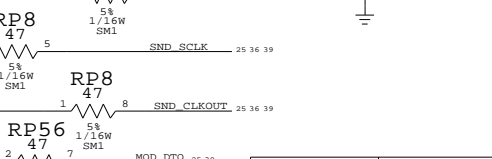
PORT D - UNUSED



PORT E - BLUETOOTH



PORT F - MODEM




HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTAG_TDO_H

INT - USB/GPIOS/I2S

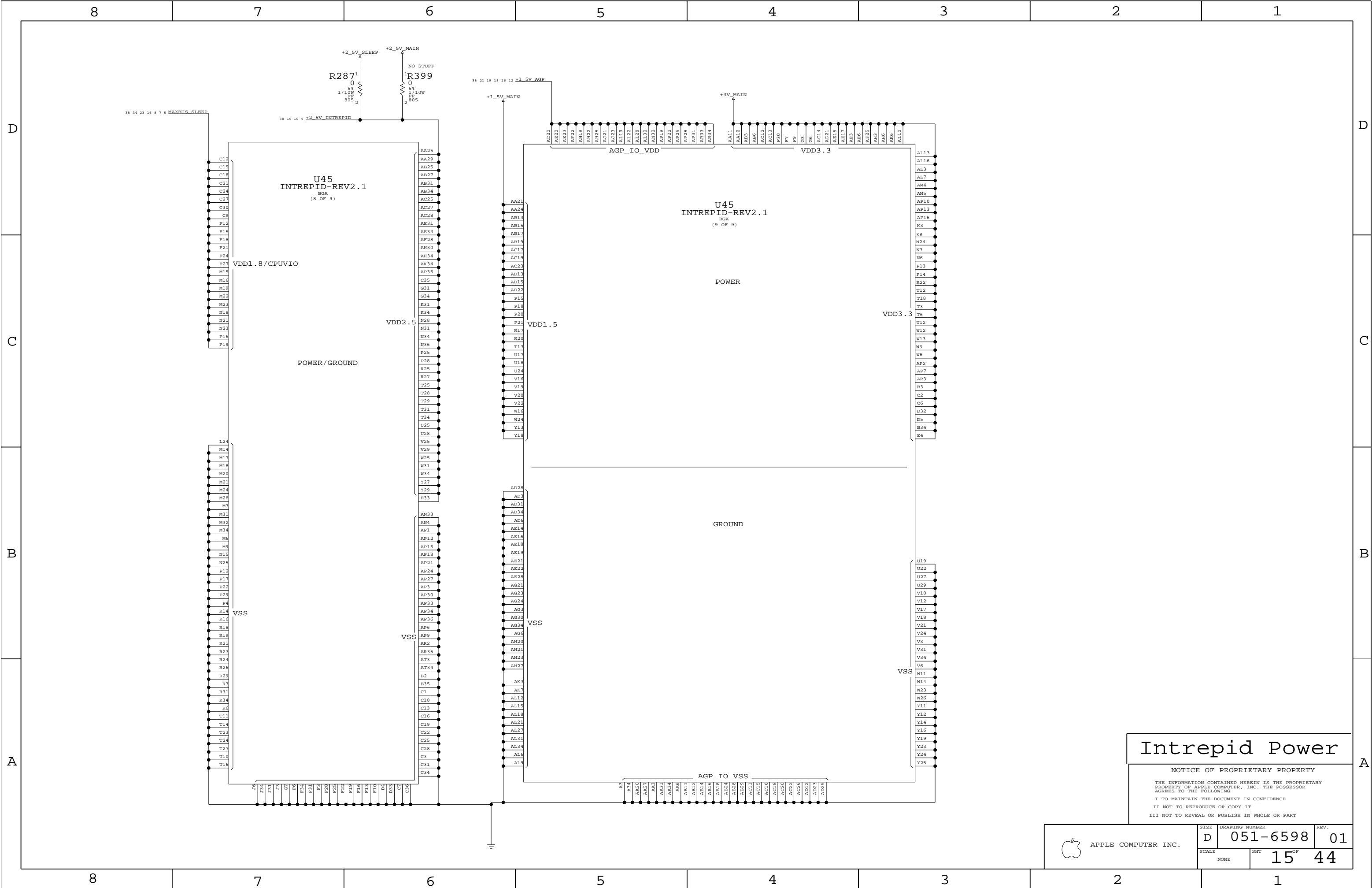
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES, METAL FILM, 10 K OHM, 5, 1/16W, 0402, SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

 APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-6598	REV.	01
SCALE	NONE	SHT	14	OF	44



Intrepid Power

NOTICE OF PROPRIETARY PROPERTY

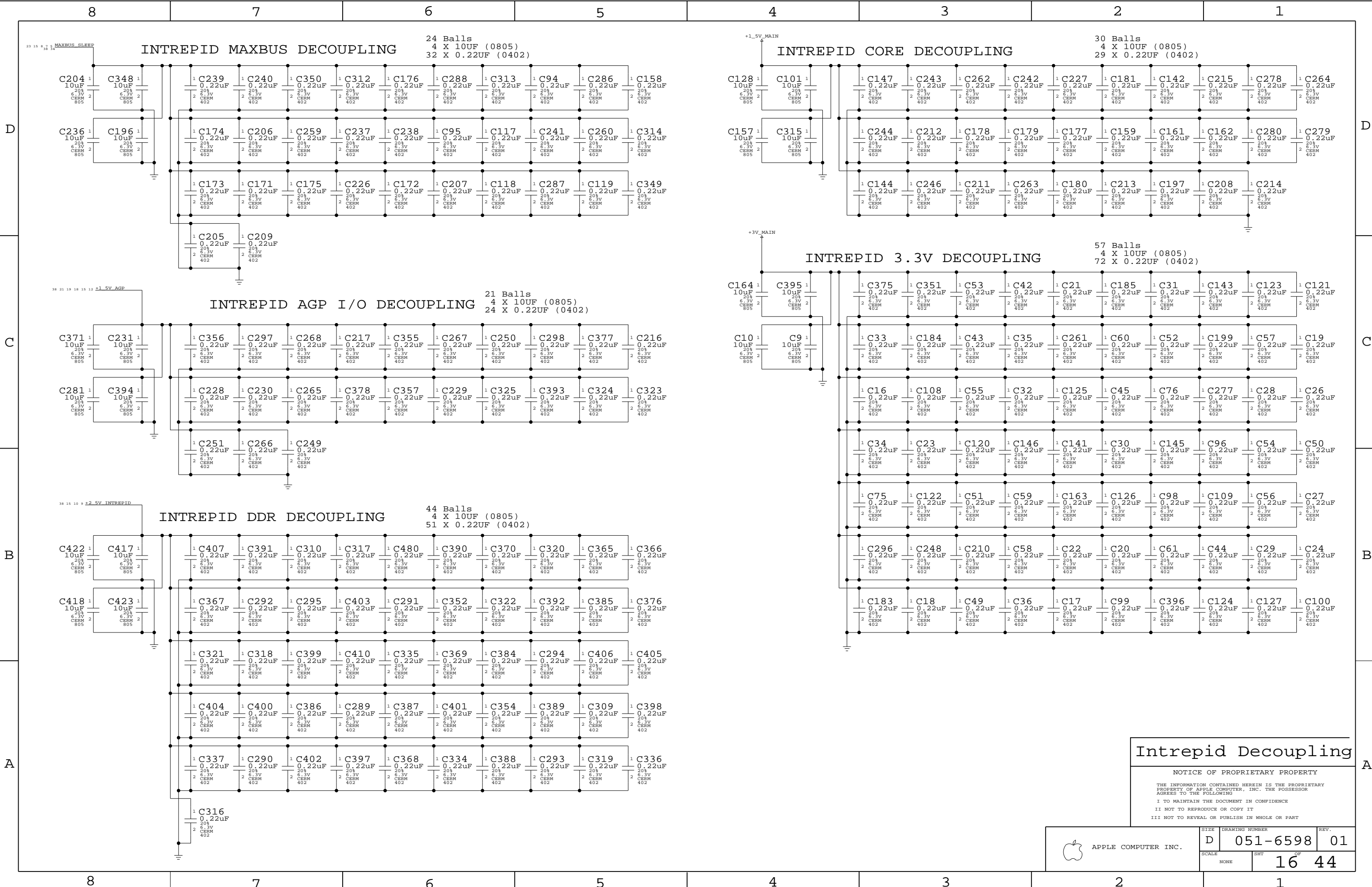
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	D	051-6598	01
SCALE	SHT		OF
	NONE		15 44



Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

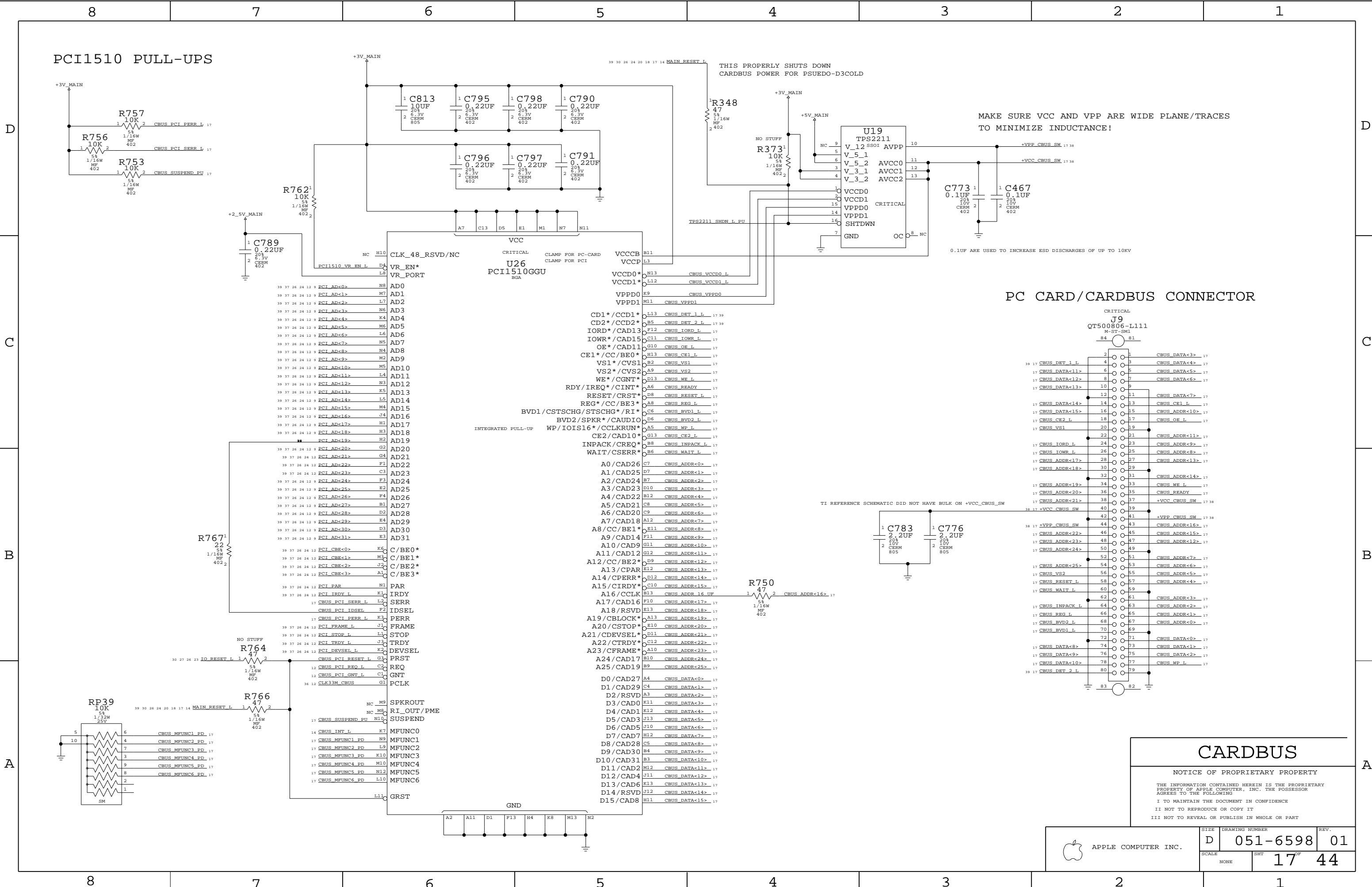
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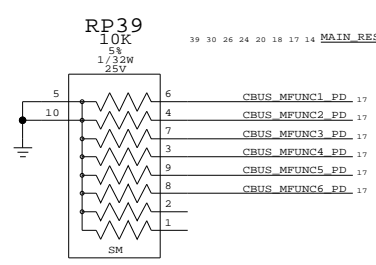
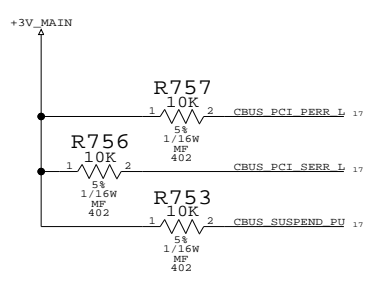
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	SHT		OF
	NONE		16 44



PCI1510 PULL-UPS

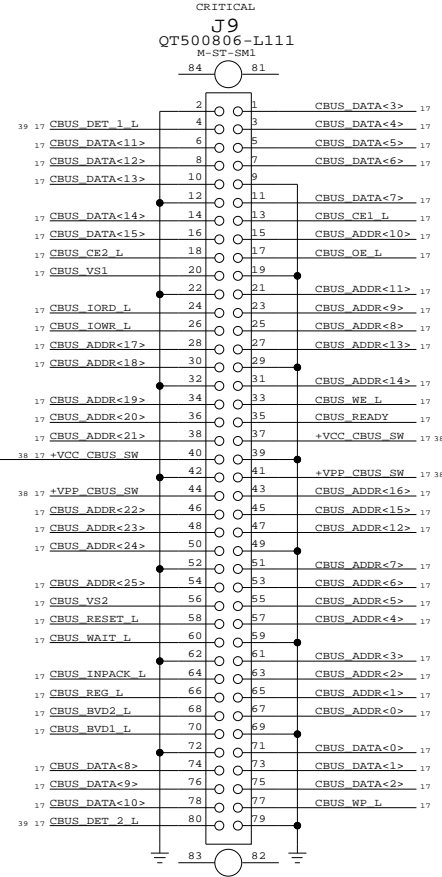


THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

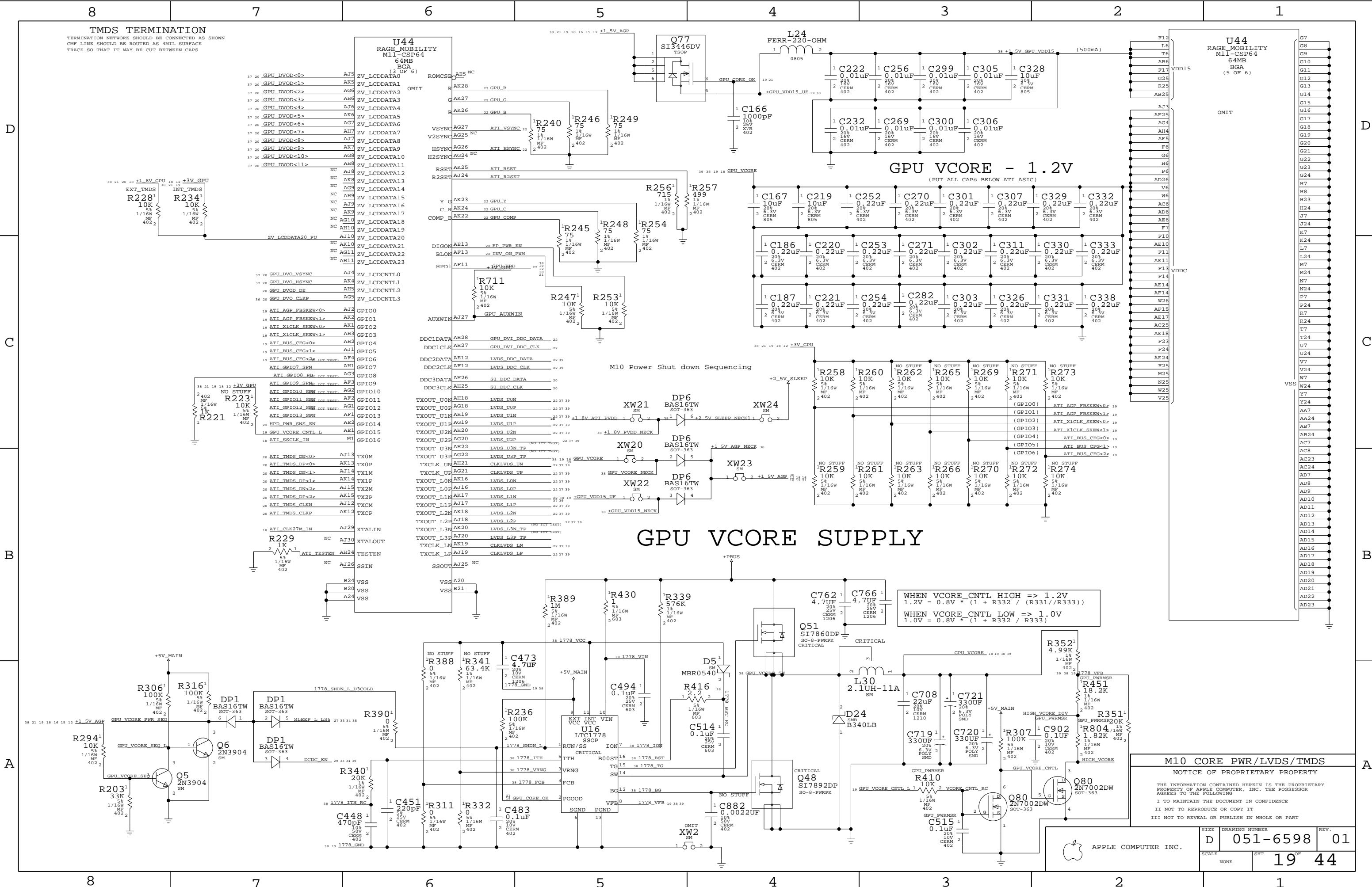
PC CARD/CARDBUS CONNECTOR



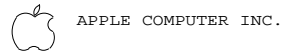
CARDBUS

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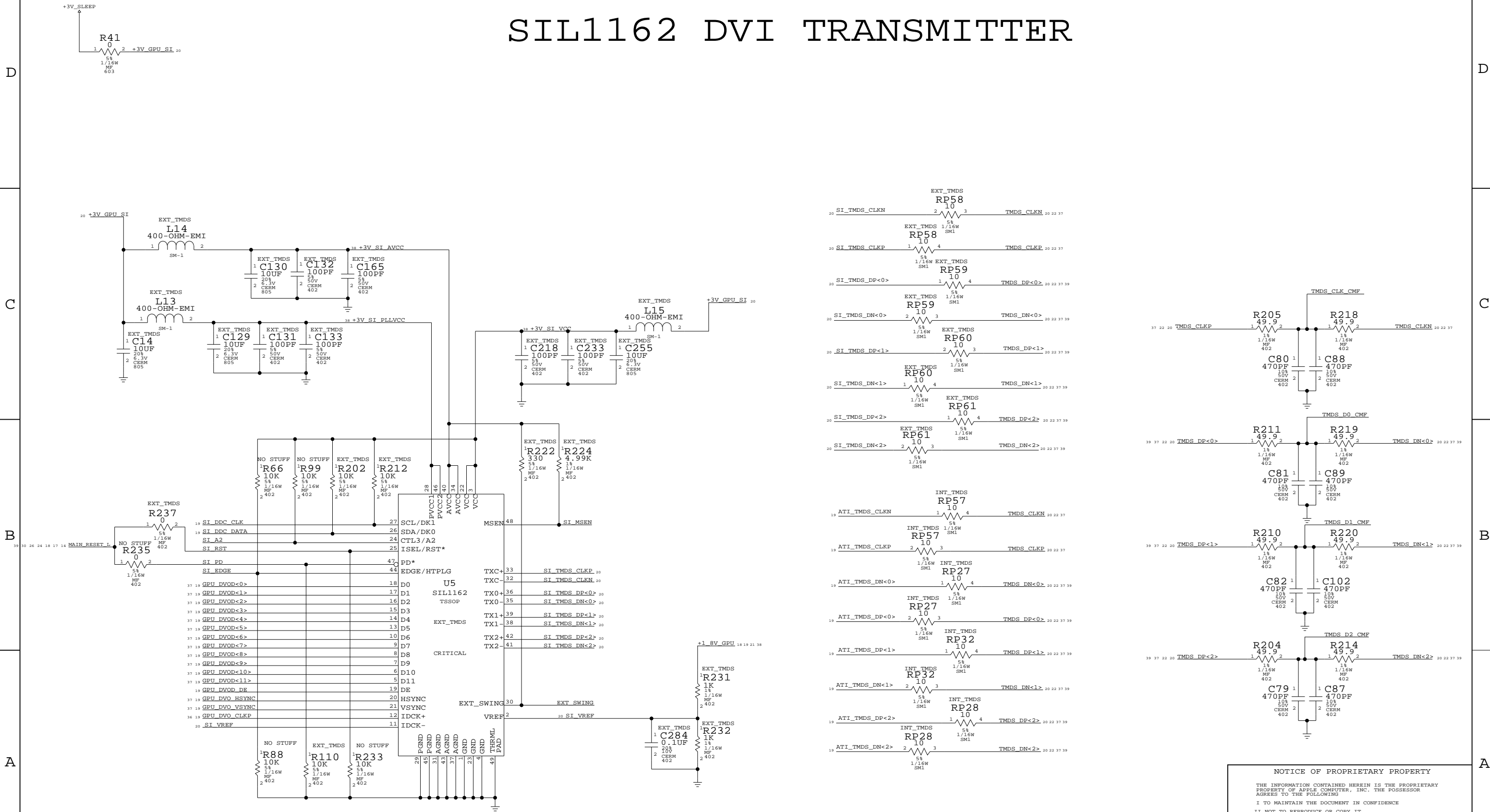
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6598	REV. 01
	SCALE NONE	SHT 17	44



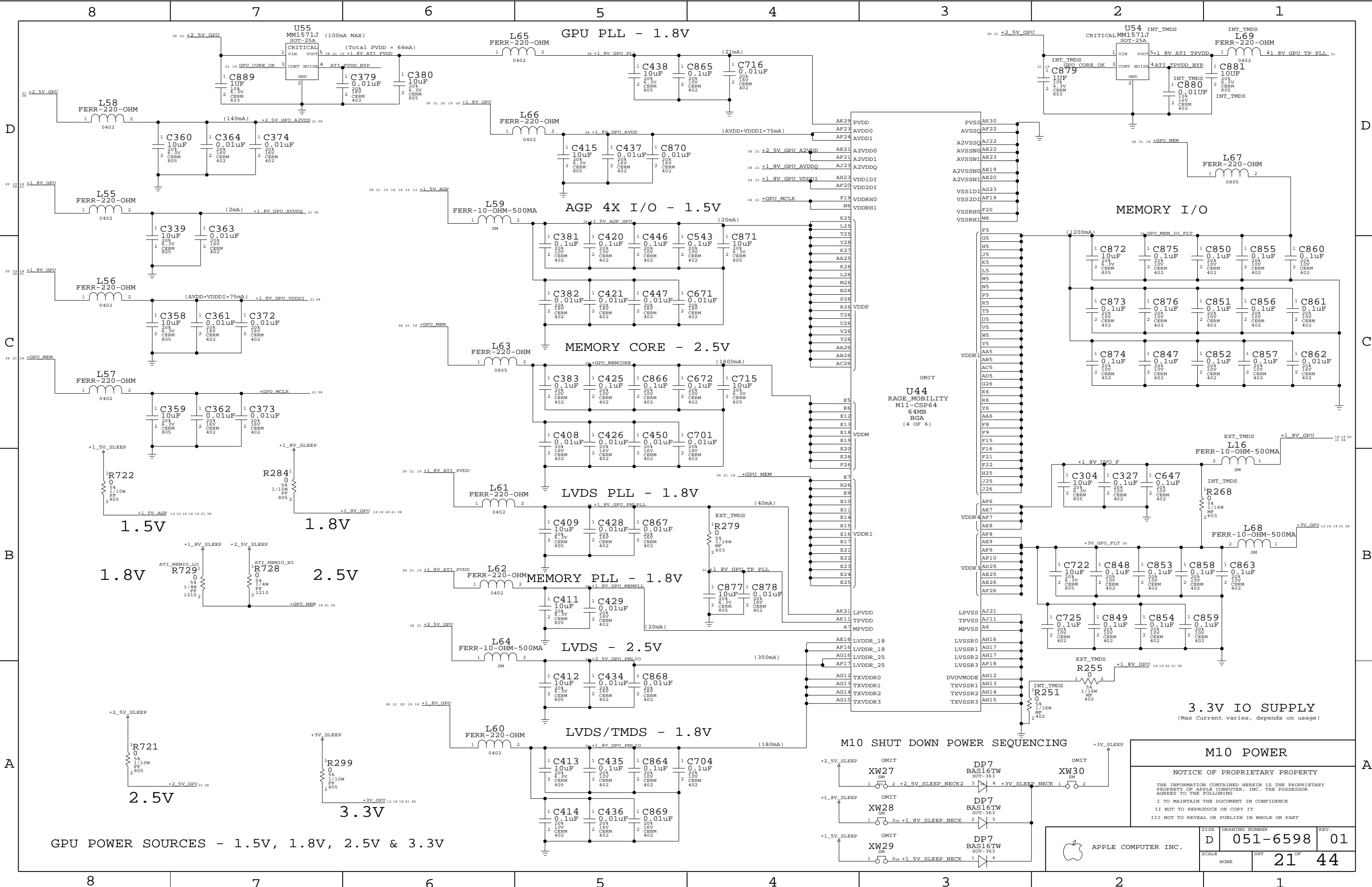
M10 CORE PWR/LVDS/TMDS		
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I NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE	SHT	19 OF 44



SIL1162 DVI TRANSMITTER

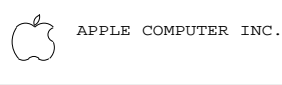


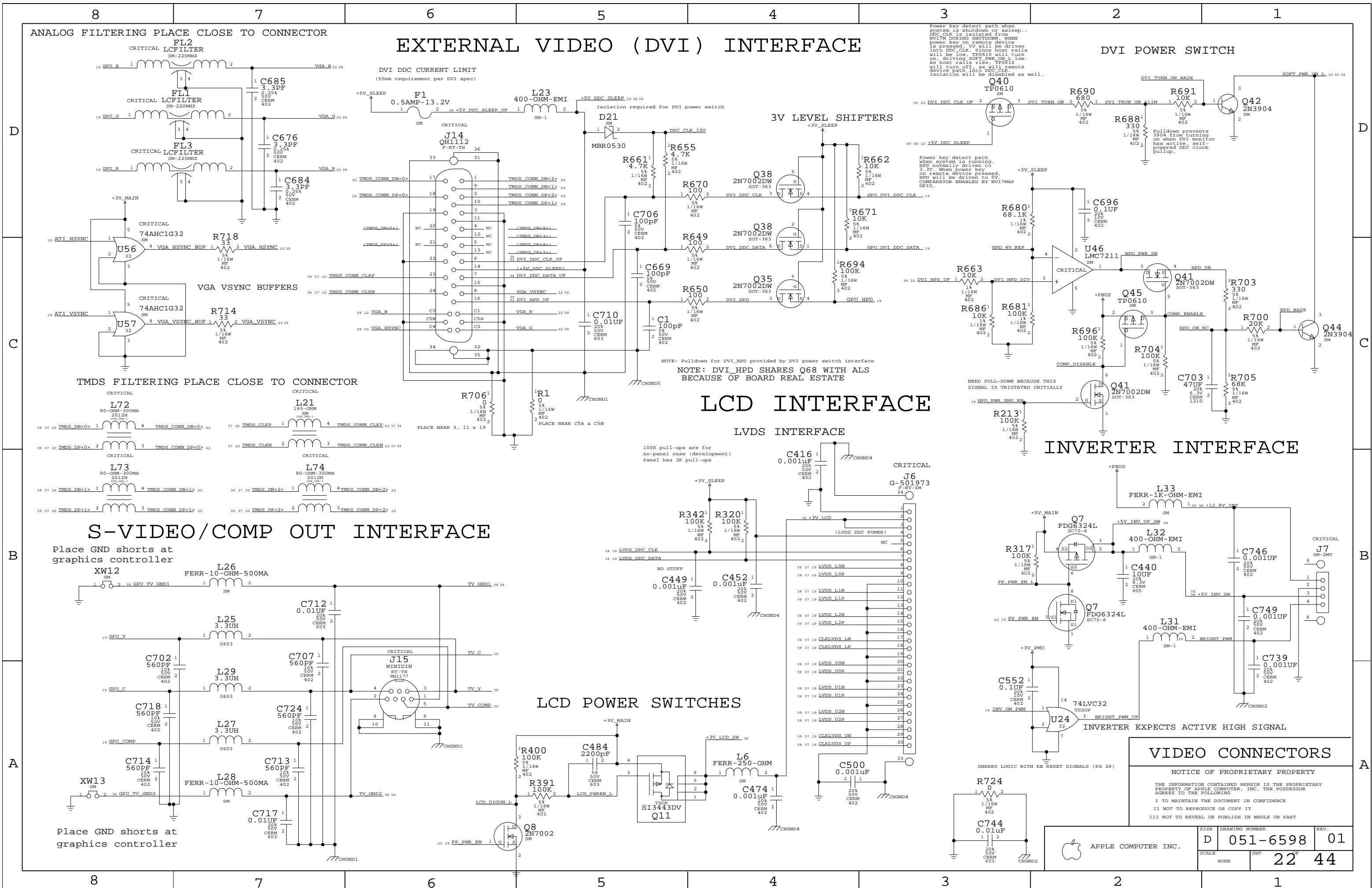
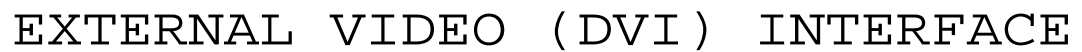
APPLE COMPUTER INC.

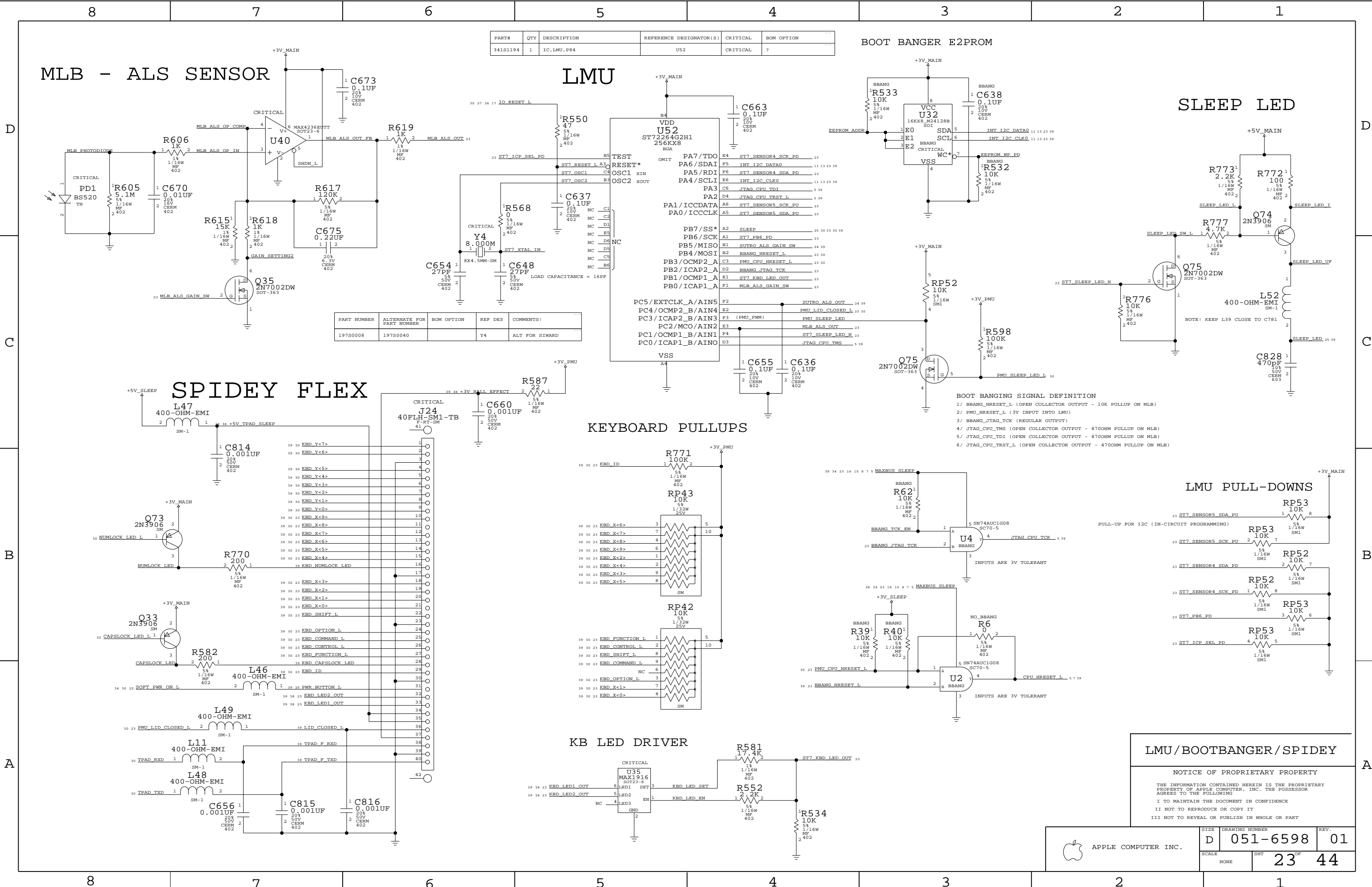


GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

M10 POWER		
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SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE	SHT	21 OF 44
NONE		

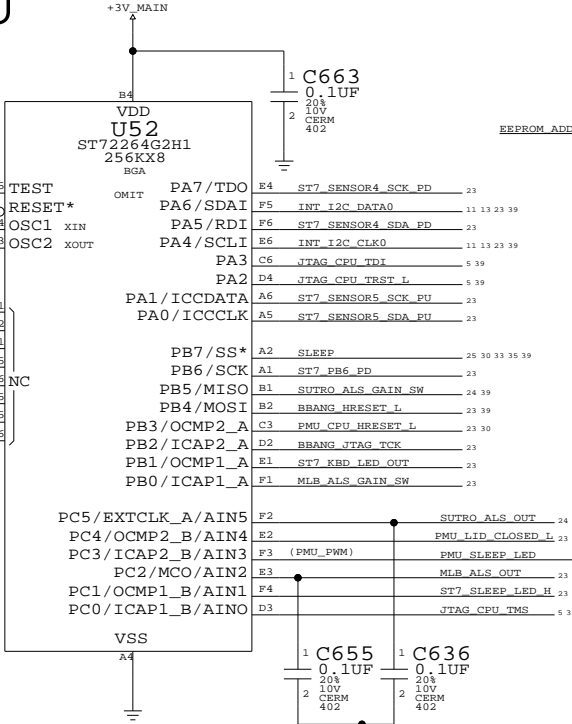






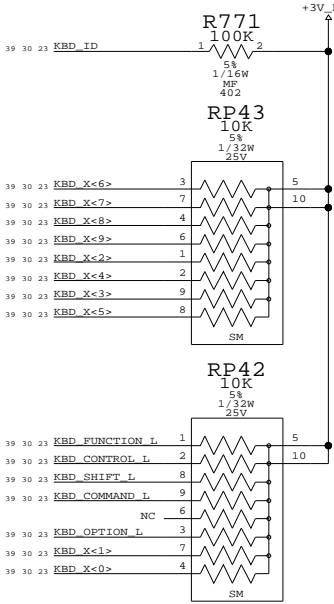
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC, LMU, P84	U52	CRITICAL	?

LMU

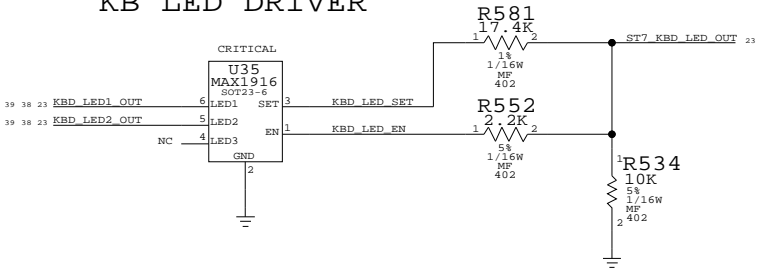


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

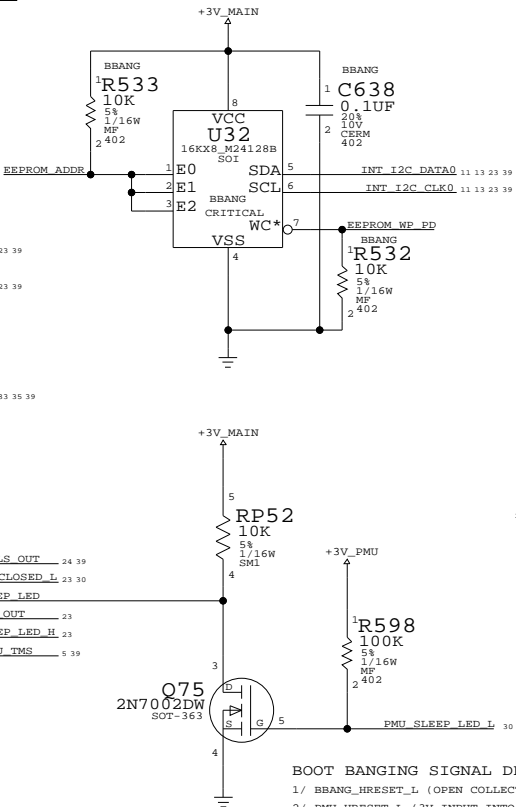
KEYBOARD PULLUPS



KB LED DRIVER

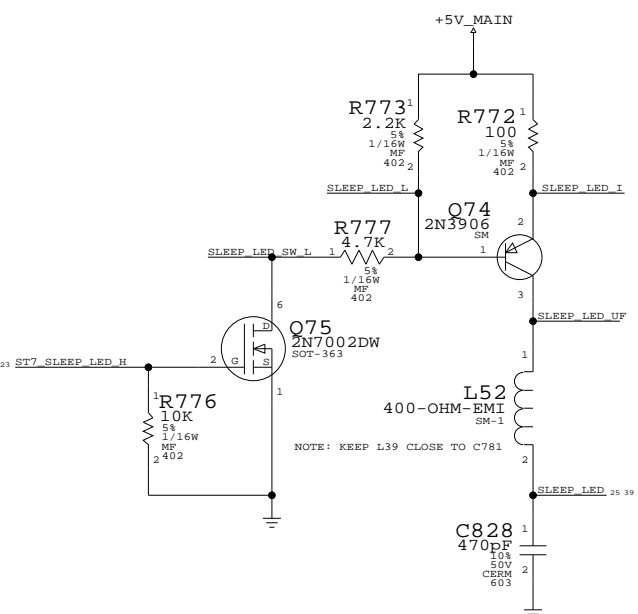


BOOT BANGER E2PROM

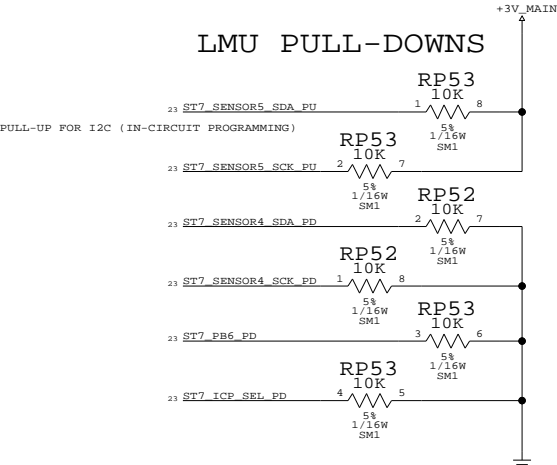


- BOOT BANGING SIGNAL DEFINITION
- 1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
 - 2/ PMU_HRESET_L (3V INPUT INTO LMU)
 - 3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
 - 4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

SLEEP LED



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

NOTICE OF PROPRIETARY PROPERTY

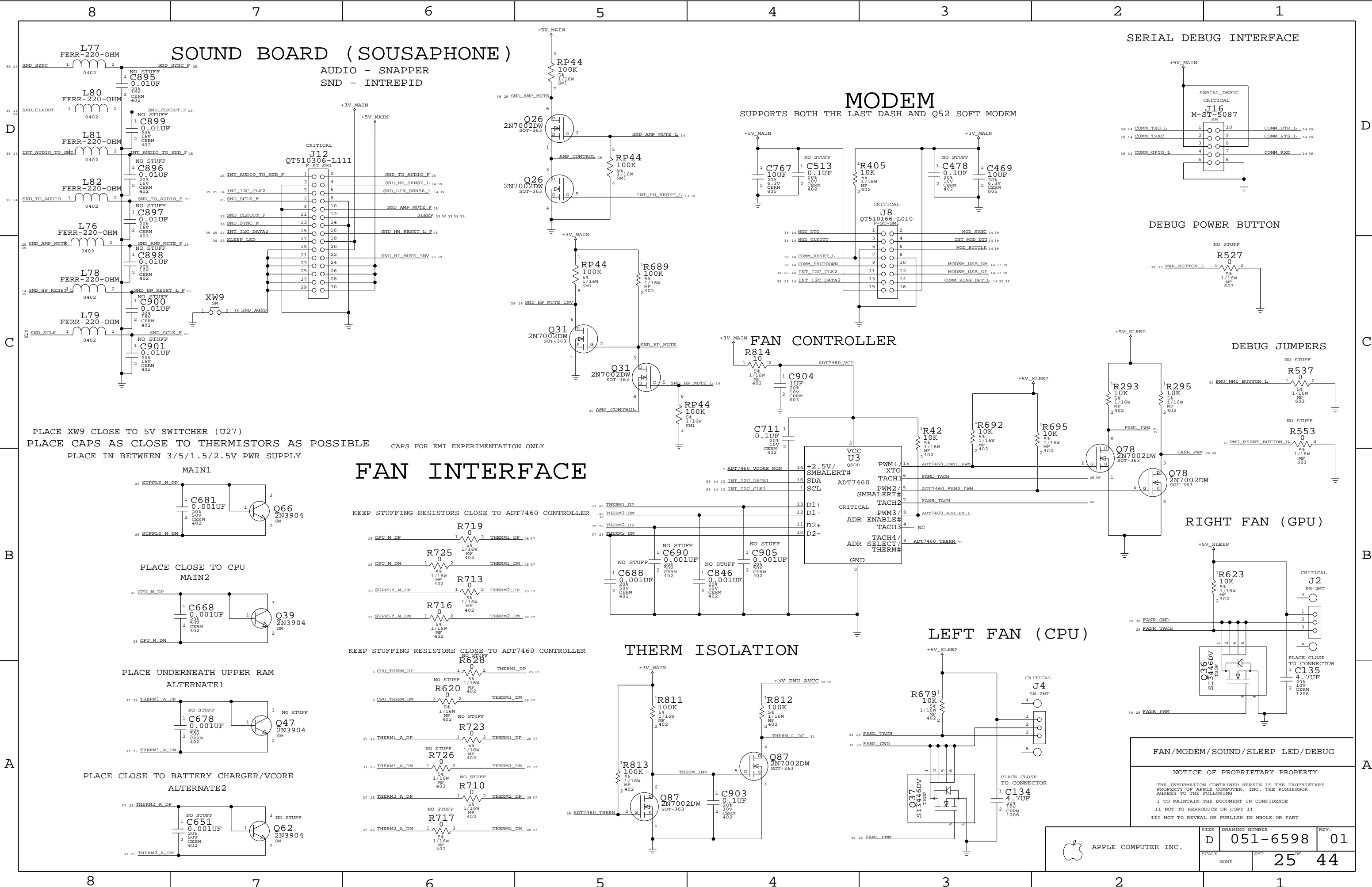
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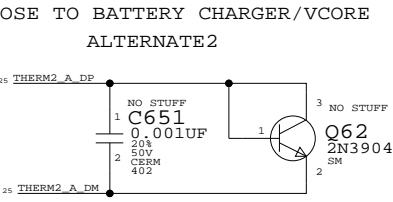
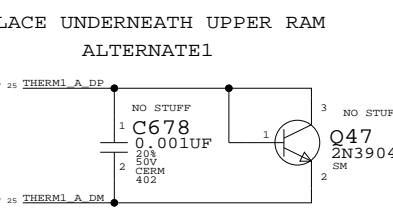
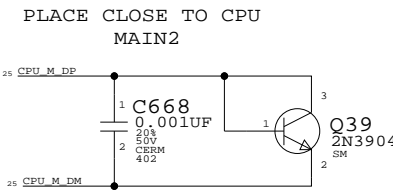
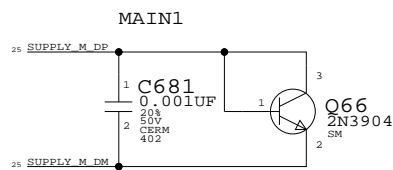
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	D	051-6598	01
	SCALE	SHT	
	NONE	23	44

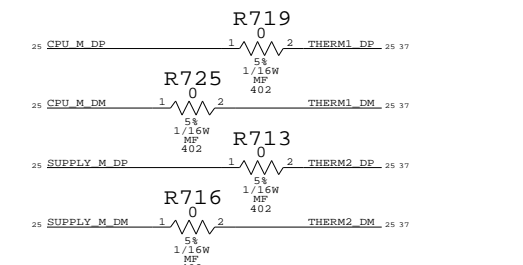


PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

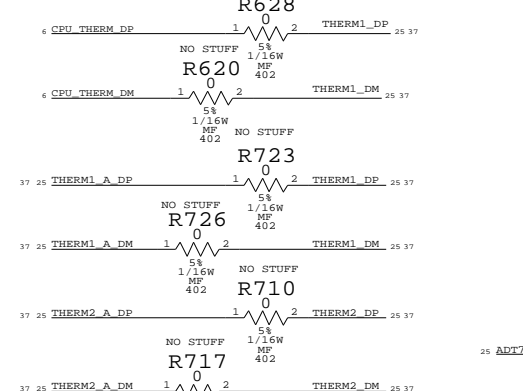


FAN INTERFACE

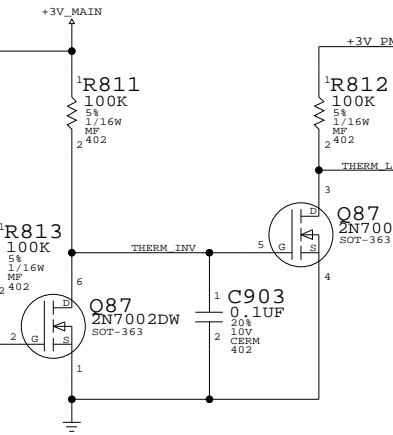
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



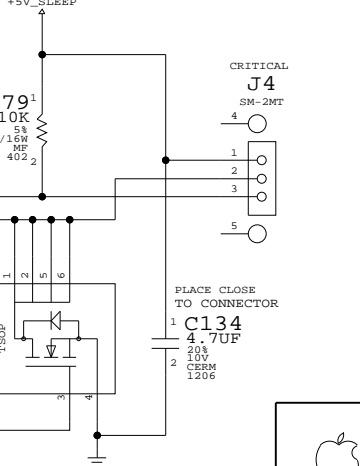
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



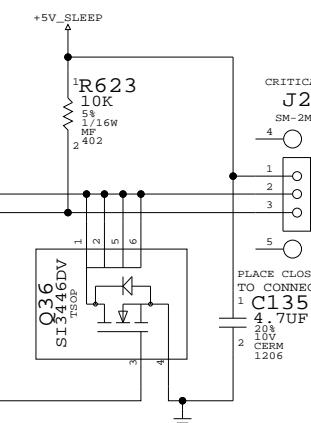
THERM ISOLATION



LEFT FAN (CPU)



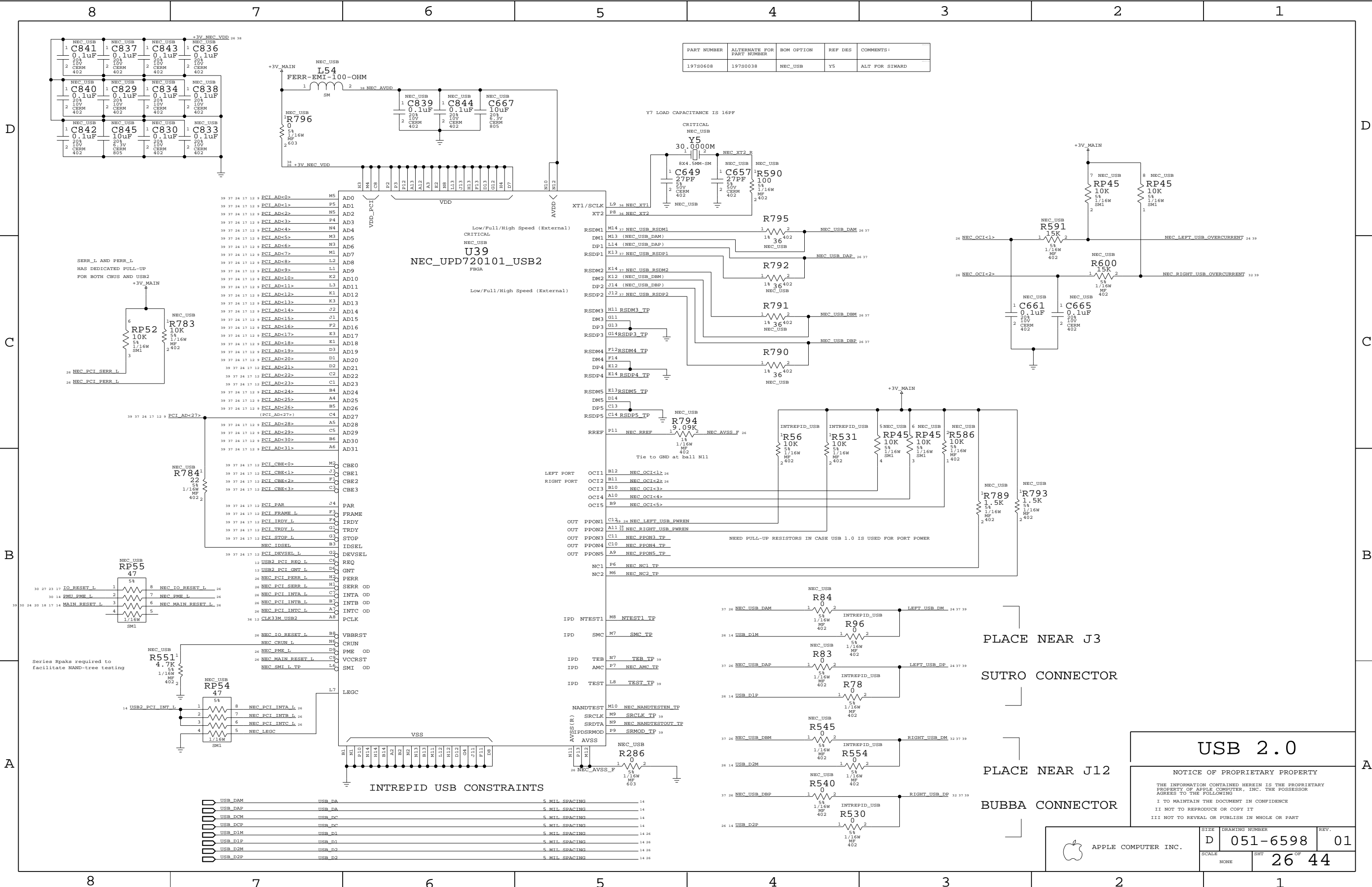
RIGHT FAN (GPU)



FAN/MODEM/SOUND/SLEEP LED/DEBUG

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	D	051-6598	01
SCALE	SHT	25	44
	NONE		



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

CRITICAL NEC_USB

Y5 30.0000M

8X4.5MM-SM

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

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NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

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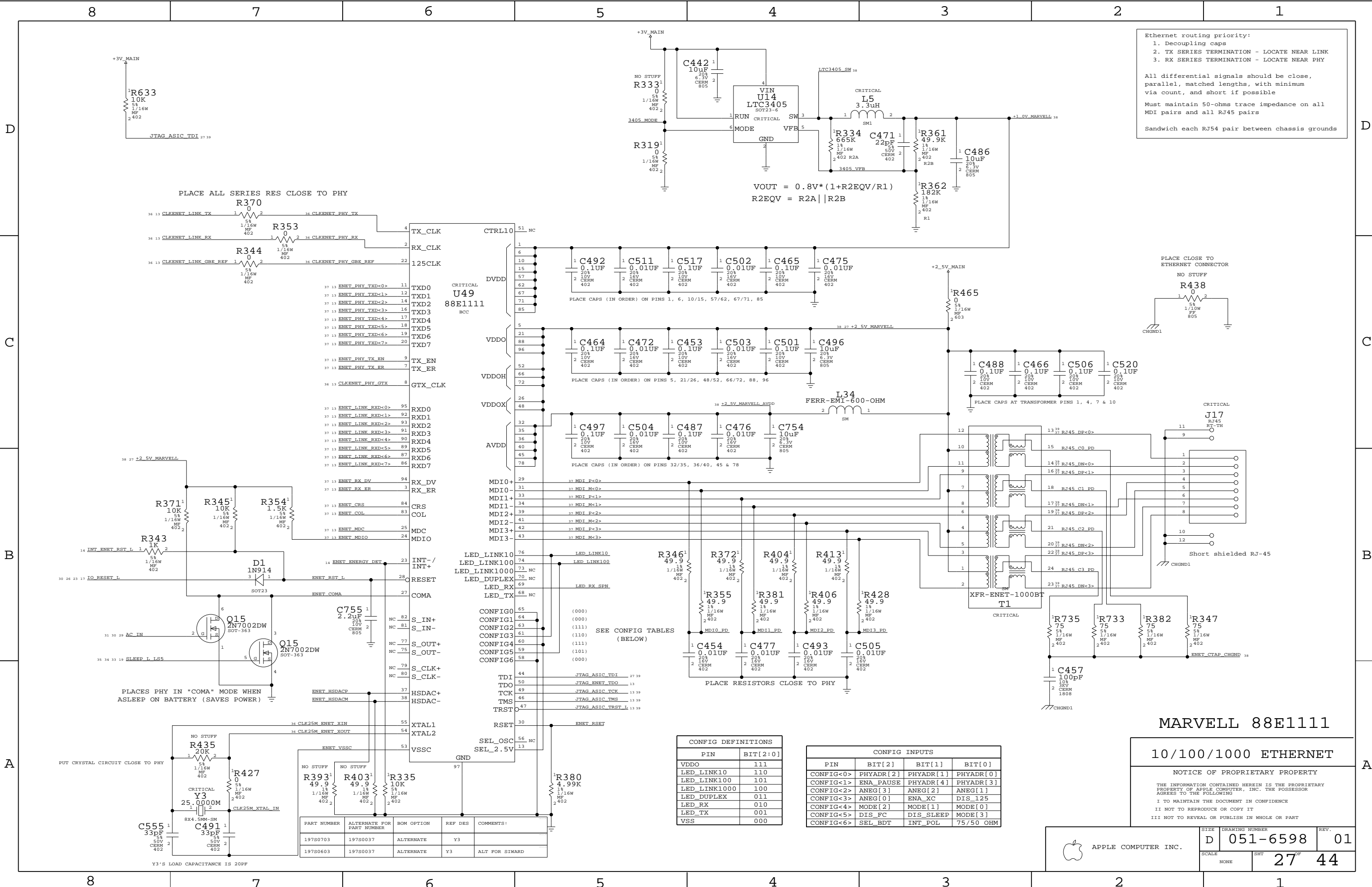


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6598 01

SCALE NONE SHT 26 OF 44



Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF

R438

CHGND1

CRITICAL

J17

RJ45

RT-TH

Short shielded RJ-45

CHGND1

MARVELL 88E1111

10/100/1000 ETHERNET

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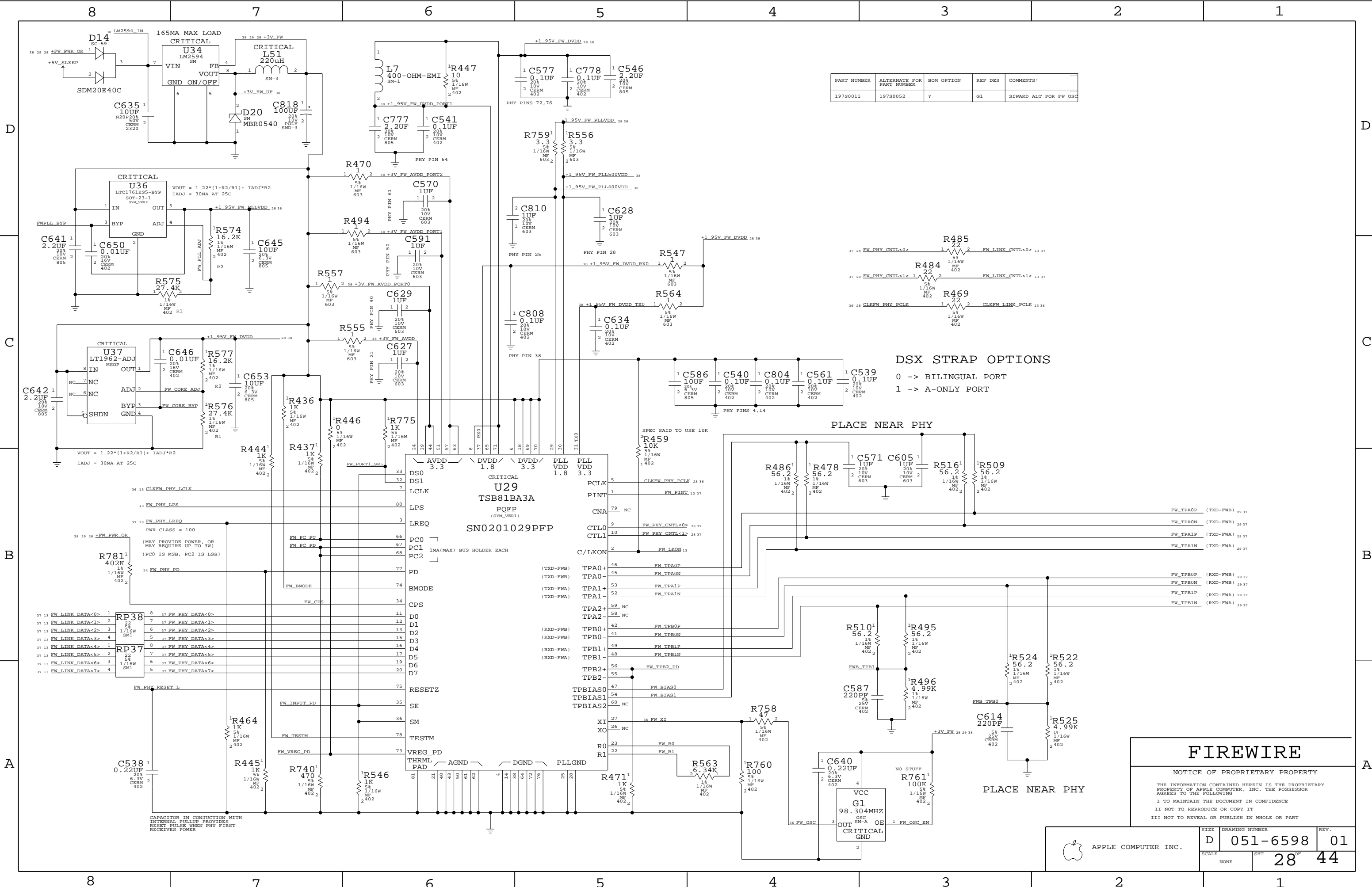
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
	SCALE	SHT	
	NONE	27	44

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	7	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

- 0 -> BILINGUAL PORT
- 1 -> A-ONLY PORT

FIREWIRE

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SCALE	SHT	
NONE	28	44

D

C

B

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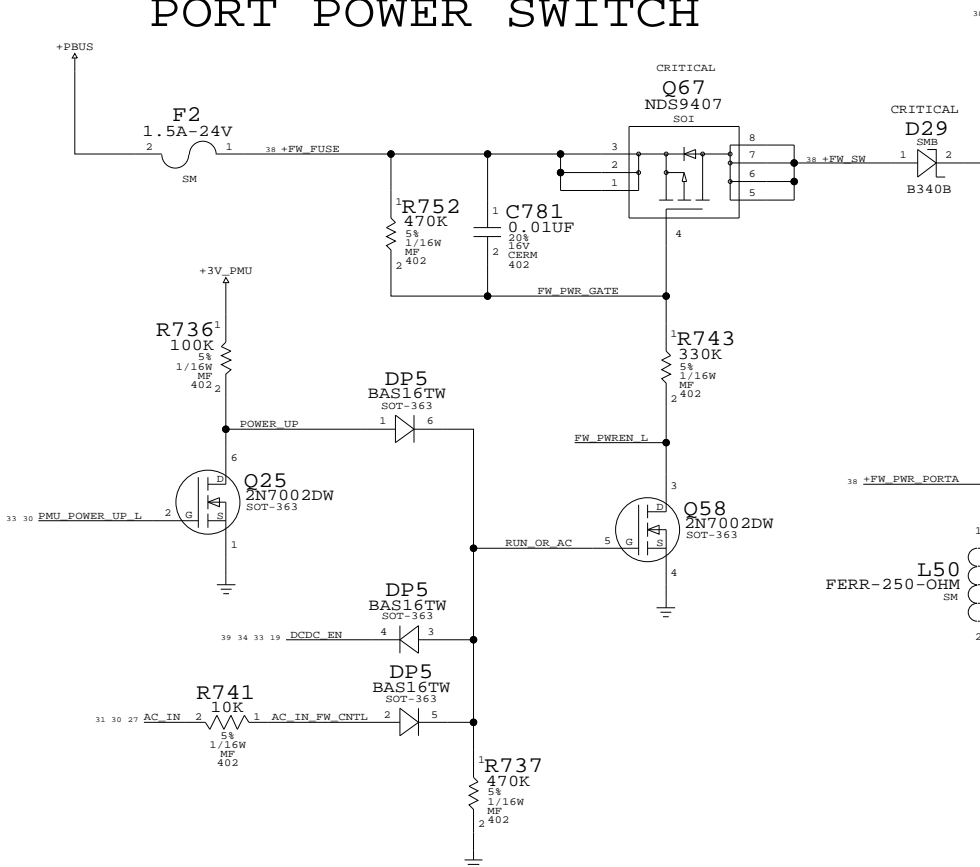
D

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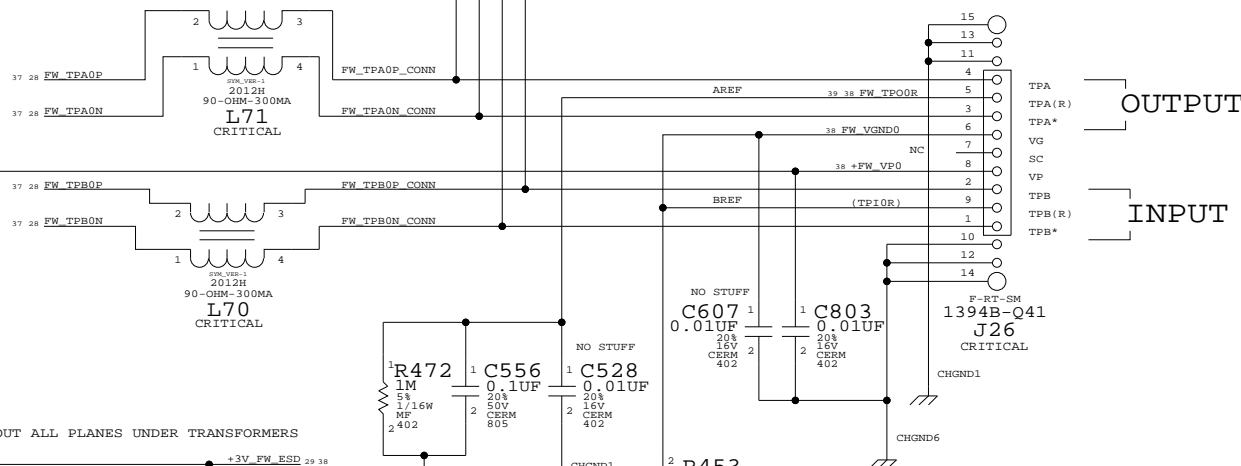
PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS
RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

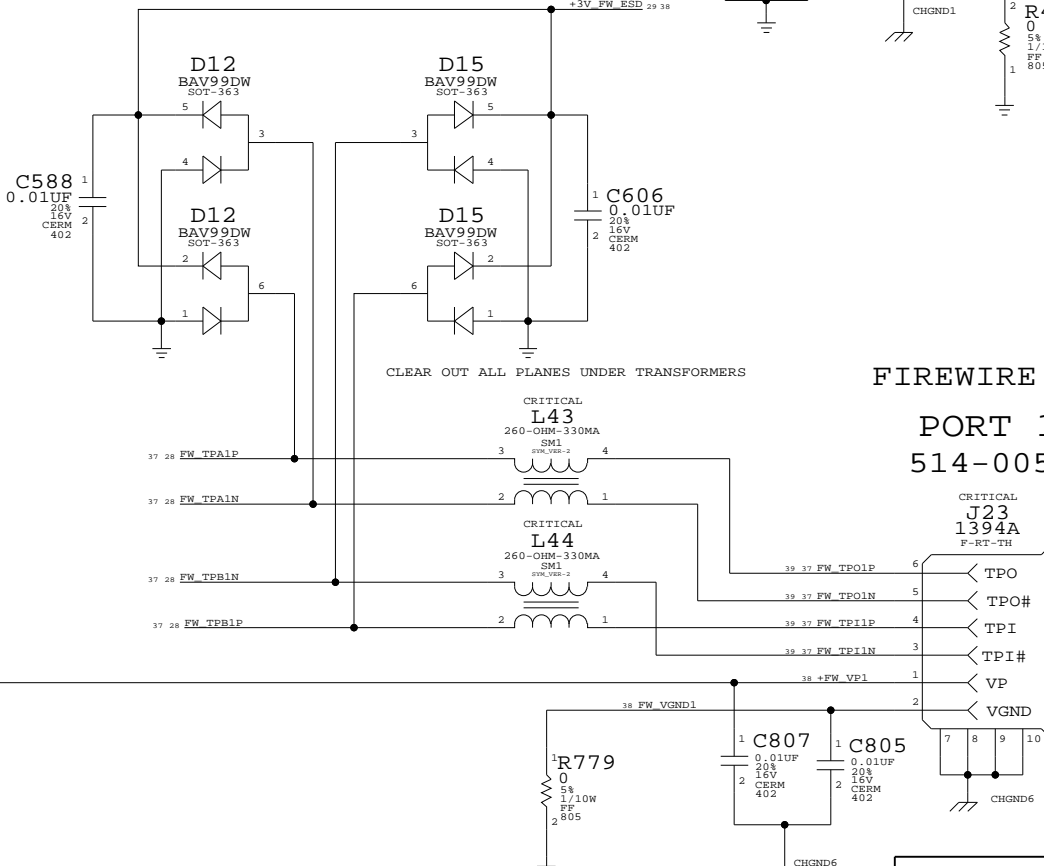
PORT 0
514S0059
FIREWIRE B - BILINGUAL



AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE
IS PLUGGED TO BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN
THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

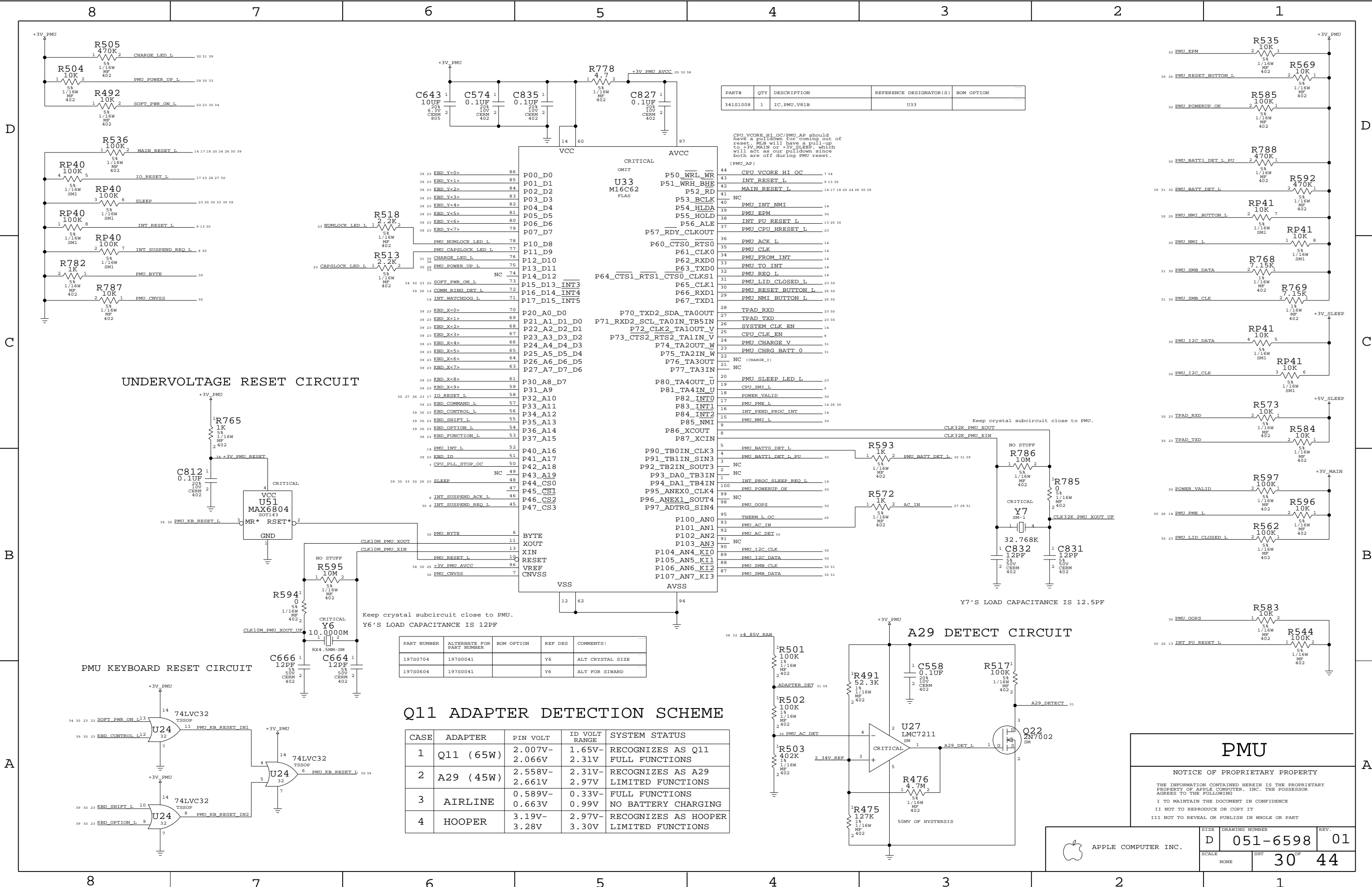
FIREWIRE A
PORT 1
514-0057



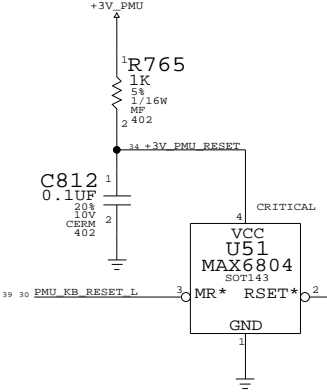
FIREWIRE PORTS

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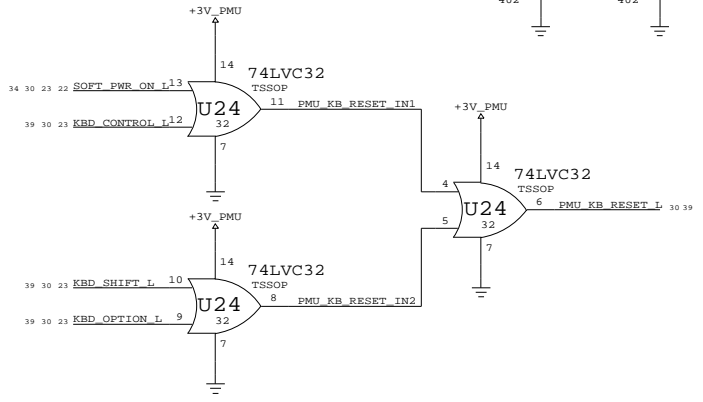
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	SCALE	NONE	SHT	29	44	



UNDERVOLTAGE RESET CIRCUIT



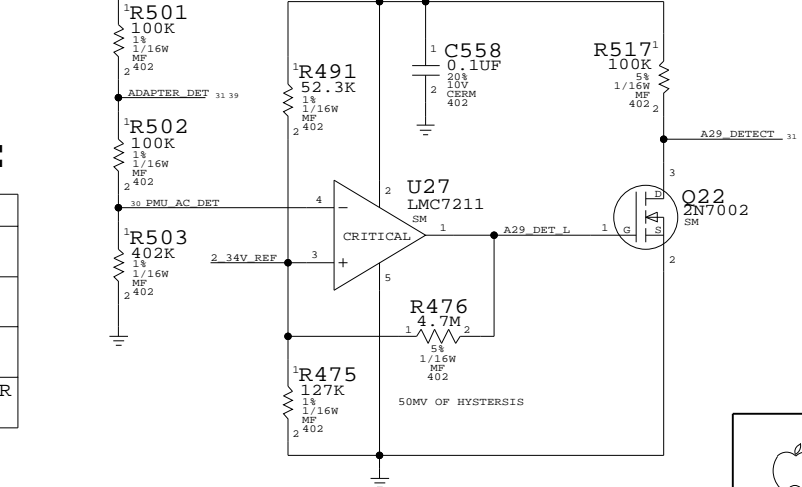
PMU KEYBOARD RESET CIRCUIT



Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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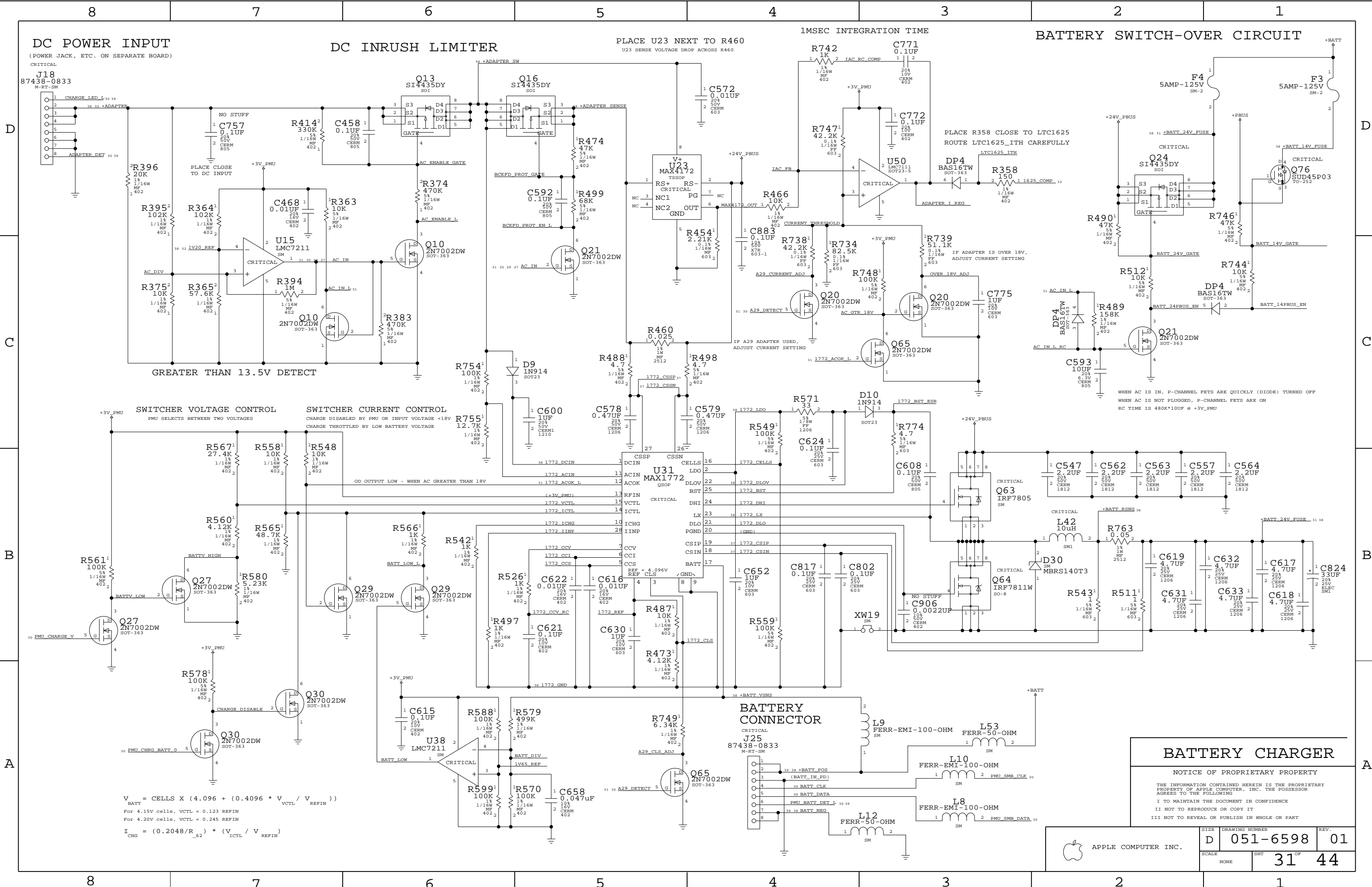
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SCALE	NONE	SHT	30	44	



$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times \frac{V_{VCTL}}{V_{REFIN}}))$$

For 4.15V cells, $V_{VCTL} = 0.123 \times V_{REFIN}$
For 4.20V cells, $V_{VCTL} = 0.245 \times V_{REFIN}$
$$I_{CHG} = (0.2048 / R_{-62}) \times (V_{ICTL} / V_{REFIN})$$

BATTERY CHARGER

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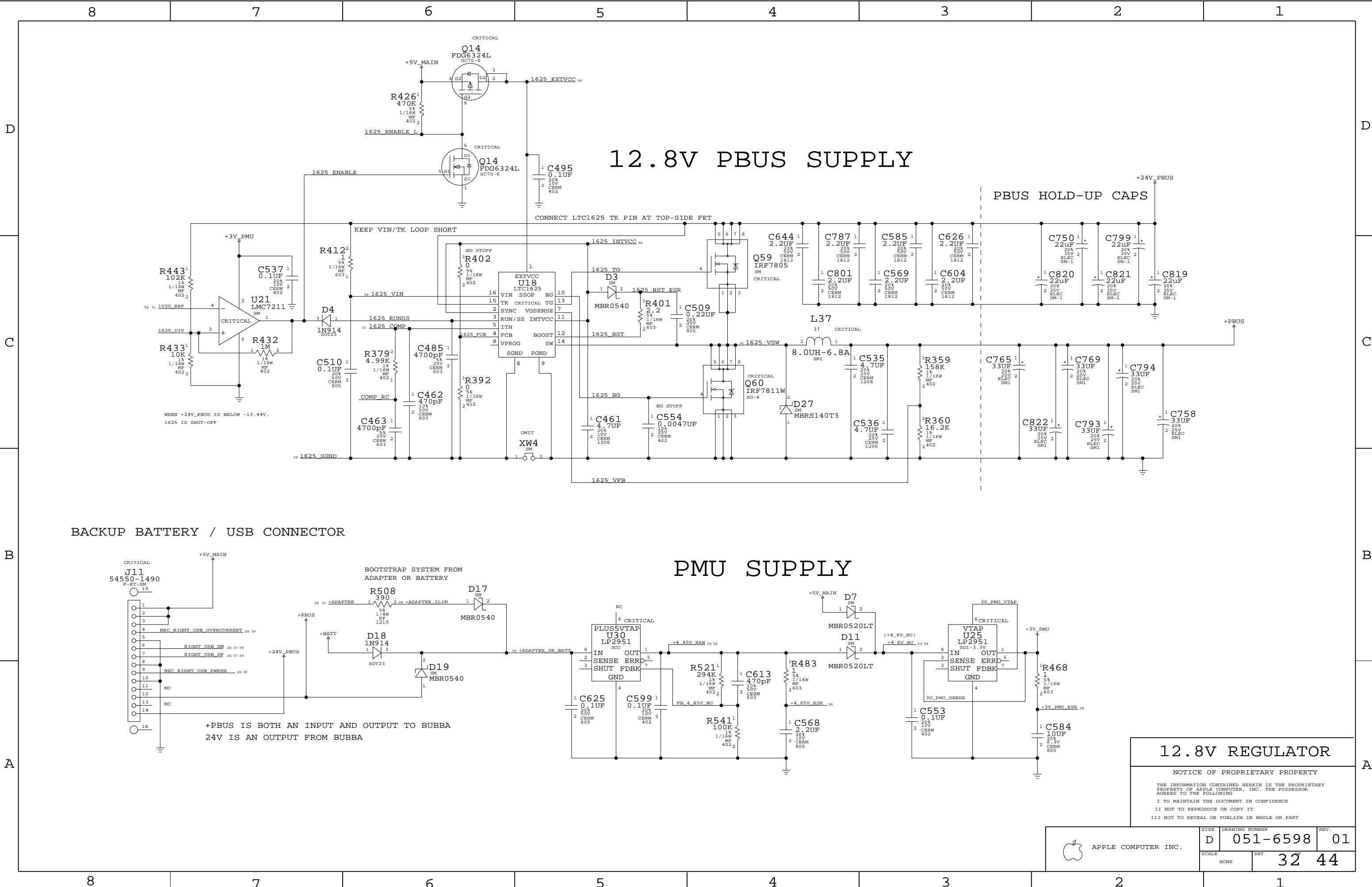
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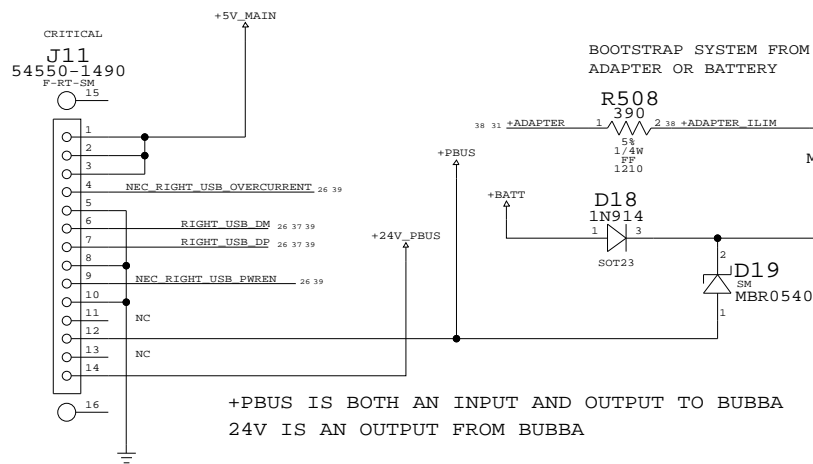
SIZE	DRAWING NUMBER		REV.
	D	051-6598	
SCALE	SHT		
	NONE	31 OF 44	



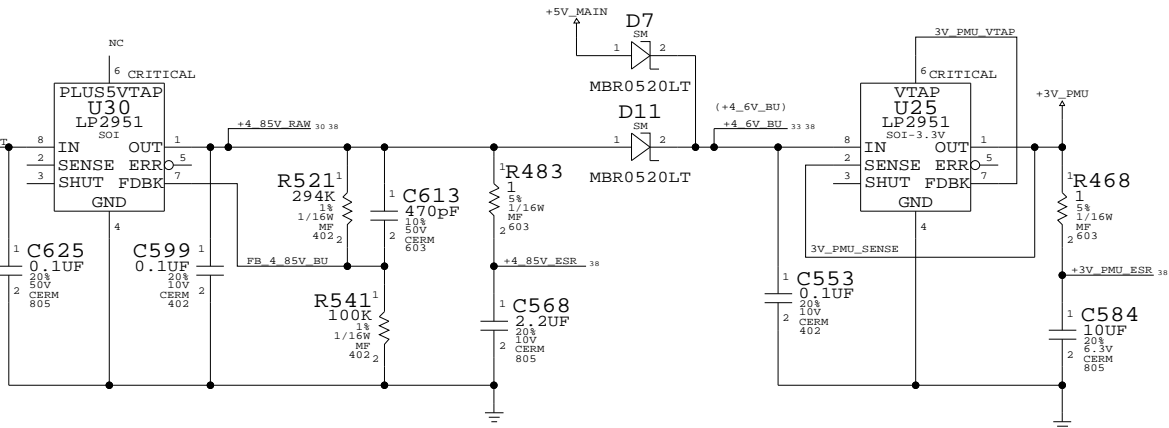
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BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

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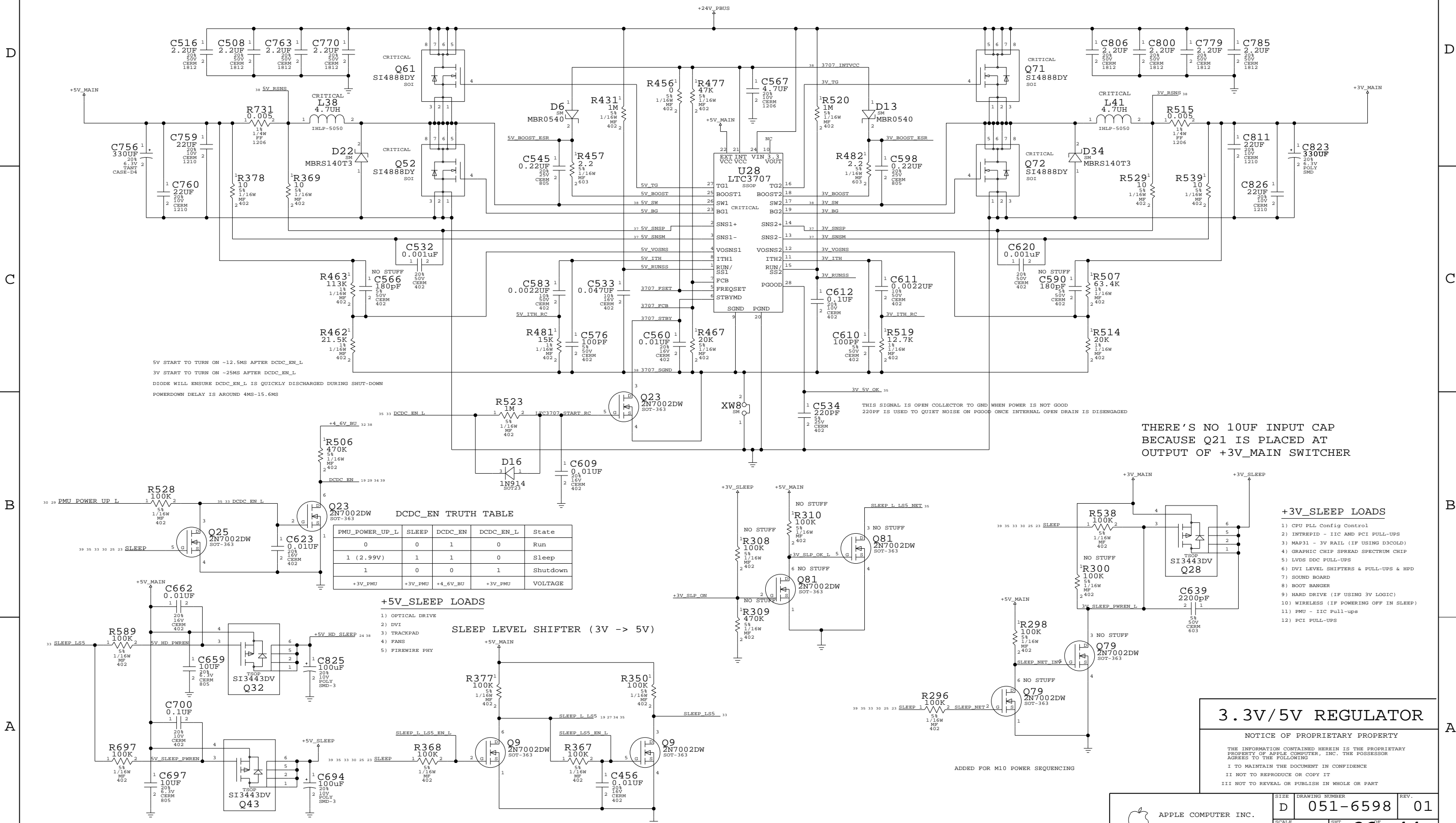
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SIZE	DRAWING NUMBER	REV.
D	051-6598	01
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NONE	32	44

3.3V/5V MAIN SUPPLY



THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

DCDC_EN TRUTH TABLE				
PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4.6V_BU	+3V_PMU	VOLTAGE

+5V_SLEEP LOADS

- 1) OPTICAL DRIVE
- 2) DVI
- 3) TRACKPAD
- 4) FANS
- 5) FIREWIRE PHY

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

- 1) CPU PLL Config Control
- 2) INTREPID - IIC AND PCI PULL-UPS
- 3) MAP31 - 3V RAIL (IF USING D3COLD)
- 4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
- 5) LVDS DDC PULL-UPS
- 6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
- 7) SOUND BOARD
- 8) BOOT RANGER
- 9) HARD DRIVE (IF USING 3V LOGIC)
- 10) WIRELESS (IF POWERING OFF IN SLEEP)
- 11) PMU - IIC Pull-ups
- 12) PCI PULL-UPS

3.3V/5V REGULATOR

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8	7	6	5	4	3	2	1
POWER NET CONSTRAINTS							
D	MAIN/SLEEP	GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
			+24V FBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+5V MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+5V SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+3V MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+3V SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
			+3V PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			+2.5V MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
C	ADAPTER		+2.5V SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+1.8V MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
			+1.8V SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+1.5V MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+1.5V SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
			+1.5V LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
			+1.5V SLEEP VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
			+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
			+ADAPTER_SM	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
			+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
B	BATTERY CHARGER		+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
			1772_PCIN	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
			1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
			+BATT_14V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
			+BATT_24V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
			+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
			+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
			1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
			1772_DEOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
A	PMU		1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
			+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+4.85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+4.6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+4.85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
			+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
			+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
B	TRACKPAD		+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	23
			+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	23
			+12.8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
			+5V_INV_UP_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
			+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
			+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
			+5V_DDC_SLEEP_UP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
			+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
			+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
			GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
C	VIDEO		GPU_TV_GND2	V			

FUNCTIONAL TEST POINTS

D

C

B

A

D

C

B

A

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NONE	39 ^{OF} 44	

[illegible]

[illegible]

[illegible]